THEORY OF OPERATION

This section of the manual describes the circuitry in the 492/492P Spectrum Analyzer. The description begins with a general and functional description related to a block diagram of the major systems within the 492/492P. This is followed with a detailed description of the circuitry within each section; for example, the Display section.

The number in the diamond refers to the corresponding schematic diagram number. Note that these same numbers are included on diagrams. Schematics of all major circuits are in Volume 2, section 8.

◇1

FUNCTIONAL AND GENERAL DESCRIPTION

What It Does

The 492/492P Spectrum Analyzer accepts an electrical signal as its input and displays the signal's frequency components on a crt. Signals can be applied directly to the RF INPUT or, if the analyzer is equipped for external mixer operation, to an external mixer, which extends the measurement range of the 492/492P.

The display of the frequency components of the input signal appears on the crt as a graph where the horizontal axis is frequency and the vertical axis is amplitude. The display can also be plotted on a chart recorder using rear-panel connectors. The 492/492P, when equipped with Option 02, can transmit the display digitally via the IEEE 488 bus.

Manual operation of the 492/492P Spectrum Analyzer is accomplished through the front-panel knobs and switches. The 492P may also be operated via the IEEE 488 bus using a straightforward language format.

How It Works

The Functional Block Diagram is located at the front of the Diagrams section. It relates the major sections in the instrument and shows the main signal paths. Refer to the diagram while reading this general description.

The 492/492P operates as a swept, narrow-band receiver. As it sweeps a range of frequencies, it moves the crt beam horizontally. When it detects a frequency component of the input signal, it deflects the beam vertically. The center

frequency of each span is set by the FREQUENCY control. The frequency range of each span is set by the SPAN/DIV control. The power level represented by the vertical deflection is set by the REFERENCE LEVEL control; this control causes the microcomputer to change the input RF attenuator or IF gain, or both, to bring signals within the display range.

First, Second, and Third Converters

In the 492/492P Spectrum Analyzer, this swept-frequency analysis is achieved with a triple-conversion superheterodyne technique.

Each of the three frequency converters consists of a mixer, a local oscillator, and appropriate filters. Only one frequency can be properly converted in each mixer and pass through all bandpass filters and reach the detector. This analysis frequency can be changed simply by changing the frequency of any of the local oscillators in the converters.

The first converter, usually referred to as the front end, converts the input signal frequency to an intermediate frequency (IF) which may be either 829 MHz or 2072 MHz depending on which band is in use. Although the internal mixer covers signals from 50 kHz to 21 GHz, an external mixer may be used for analysis through the millimeter wavelengths (unless this capability is deleted by Option 08). If the 492/492P is equipped with Option 01, a preselector and a lowpass filter attenuate unwanted signals when the internal mixer is used. This prevents most images and spurious responses.

There are actually two second converters in the 492/492P; the appropriate converter is selected automatically for each band so the input frequency range does not overlap the first IF frequency. Each second converter has its own local oscillator (LO), mixer, and filters. Both convert the signal to 110 MHz and send it to the third converter.

The third converter amplifies the 110 MHz IF signal and converts it to the final intermediate frequency of 10 MHz. The third converter passes the signal to the IF section for detection.

IF Section

The IF section analyzes how much power is present in the frequency component that has been converted to 10 MHz. Three functions are performed here:

1) weak signals can be amplified by a set of switchable amplifiers so that they may be analyzed. By amplifying the signal, the vertical window (dynamic display range) is shifted up or down. The REFERENCE LEVEL control selects the gain (and input RF attenuation as a pair) to frame this window;

2) the signal is bandpassed by any of several 10 MHz bandpass filters selected by the RESOLUTION BANDWIDTH control. The greater the selectivity, the better two closely-spaced signals can be resolved, but narrow bandwidths require longer sweep times. The microcomputer selects the best combination of bandwidth and sweep time, unless overridden by the operator;

3) the remaining signal is detected by a combination of a logarithmic amplifier and a linear amplitude detector. The output of this combination is a voltage that corresponds to the signal strength in decibels. This amplitude detector output is sent to the vertical channel of the display section to show the strength of the particular component.

Display Section

The display section draws the display on the crt screen. Vertical deflection of the beam is increased as the output of the amplitude detector increases. The horizontal position is controlled by the frequency control section and corresponds to the frequency analyzed at that instant. As the 492/492P sweeps from low frequencies to high frequencies during its analysis, the beam is swept from left to right. Any time a signal is encountered during the analysis, a vertical deflection shows the strength of the signal at the horizontal position corresponding to the frequency. The result is a display of amplitude as a function of frequency.

The video amplifier scales the output of the detector for vertical deflection in dB/div or performs a log/linear conversion, depending on the vertical display mode. The video processor filters the video if either the wide or narrow filter is selected.

The display section displays control settings on the crt based on data from the microcomputer.

The sweep is often rapid enough to give a flicker-free display, but at times the sweep must be slowed below the flicker rate. With Option 02, the display can be recorded and refreshed at a flicker-free rate by the digital storage section. The 492/492PP can read out the display data from digital storage through the IEEE 488 interface.

Frequency Control Section

The instantaneous frequency being analyzed is controlled by the frequencies of the local oscillators. To analyze another frequency, a local oscillator frequency is changed so that the new frequency is converted by the three converters to 10 MHz and passes through the IF section. Each converter section has its own local oscillator. Only the local oscillators of the first two converters are changed to vary the frequency being analyzed; the 3rd LO remains fixed.

The 492/492P periodically sweeps and analyzes a frequency range centered about a frequency set by the FREQUENCY knob. The FREQUENCY knob tunes the first and second local oscillators. The analyzer sweep is generated by the sweep generator and the span attenuator. As the sweep generator sweeps through its range, the trace is deflected across the screen on the front panel. The frequency sweep is controlled by the span attenuator, which scales the sweep according to the current SPAN/DIV. The output of the span attenuator drives the 1st LO to sweep wide spans and the 2nd LO to sweep narrow spans. Option 03 adds phase-lock circuitry to stabilize the 1st LO in narrow spans.

If the 492/492P is equipped with Option 01, the frequency control section tunes the preselector to track the signal frequency being detected.

Digital Control Section

Internal functions are controlled from the front panel through a microcomputer. An internal instrument bus allows communication between the microcomputer and all parts of the instrument. Front-panel control data goes to the microcomputer on this bus. The microcomputer controls circuit functions such as; the span attenuator, IF gain, and crt readout on this bus. The microcomputer also receives information from circuit functions such as, the sweep and phase lock circuitry on this bus.

The 492P may be controlled remotely through the IEEE 488 bus, which interfaces to the microcomputer through a General Purpose Interface Bus (GPIB) board. The IEEE 488 connector is located on the rear panel of the instrument. The control language corresponds closely to front-panel operation of the 492P.

Other Systems

The power supply system provides regulated dc power for all parts of the instrument. The switching supply is capable of regulation over wide line frequency and line voltage ranges.

The cooling system consists of an intake on the bottom of the case, air passages within the instrument, a fan, and a rear panel exhaust. Air is routed to all sections of the instrument in proportion to the heat generated by that section. Internal temperature rise is small for reliable operation.

Signal, power, and control connections between sections are accomplished by a mother board distribution system. Most circuit boards plug onto the mother board from the top side. Components on the RF deck underneath the mother board are also connected to the mother board through smaller connectors.

For Further Information

The systems in the 492/492P are described in nine sections as shown by the Functional Block Diagram. Nine block diagrams representing these systems follow the Functional Block Diagram.

For more detailed information, the instrument is divided into circuit diagrams for each assembly or part of an assembly. Each schematic is accompanied by a detailed block diagram and a parts location illustration. These are printed in the Diagrams section with look-up tables to aid in finding components on either the schematic or parts location illustration.

DETAILED DESCRIPTION

The following description is arranged by sections or systems; such as 1st Converter, 2nd Converter, etc., followed by circuit analysis of the circuits within that section. Each system/section is introduced with a description of the system using the block diagram found in the Diagrams section of the manual. This is then followed with a description of each circuit board or major circuit within the system.

⟨2⟩
1ST CONVERTER CIRCUITS

The 1st Converter mixes the incoming RF signal with a tunable local oscillator signal to produce intermodulation products. All of these are filtered out except the 2072 MHz and 829 MHz IF signals, which are applied to the 2nd Converter circuit.

The 1st Converter consists of the following major segments:

1) the RF Attenuator, which sets the input power to the analyzer;

2) the Preselector (Option 01 only), which provides the selectivity required to eliminate spurious responses and image frequencies;

3) the 1st LO (Local Oscillator), which provides a tunable signal for the 1st Mixer;

4) the Power Divider, which splits the signal from the 1st LO for application to the 1st LO OUTPUT front-panel connector, and 1st Mixer. (The 1st LO signal passes through the Phase Gate to the 1st Mixer if Option 03 is included);

5) the Phase Gate, which couples a portion of the oscillator signal to a phase gate that compares the phase of the oscillator signal against a strobe signal from the phaselock system;

6) the Transfer Switch, which permits the use of an external mixer with the analyzer;

7) the Filter and Diplexer circuits, which select only the 2072 MHz and 829 MHz IF signals for application to the 2nd Converter;

8) the RF Interface circuits, which select the input RF attenuation, control the selection of the IF frequency (2072 or 829 MHz), and control the transfer switch.

The input RF is fed through a 0 to 60 dB decade attenuator to the 1st Mixer (if Option 01 is not included) via a 3 dB attenuator. The attenuator matches mixer impedance and protects the mixer diodes from spurious or static signals.

The 1st LO feeds signal to the Mixer in one of two ways: directly from the Power Divider, or through the Phase Gate and Bias Return if Option 03 is installed. (The Phase Gate and Bias Return stages incur very little loss.) The Phase Gate couples off a small amount of signal (approximately 0 dBm) to compare with a strobe signal from the phaselock system. The output is an error signal that is used by the phaselock system for determining the FM tuning current for the 1st LO. The Bias Return provides high-pass filtering for the 1st LO and a dc return for the 1st Mixer diodes.

The current tuned 1st LO output is mixed with the incoming RF, and the IM (intermodulation) products are routed through the Transfer Switch to the 2.072 GHz Directional Filter. (Option 08 deletes the Transfer Switch.) This filter is broadband, and provides a constant match to the 1st Mixer output at all frequencies. The filter couples the 2.072 GHz IF to the 2nd Converter through a 4.5 GHz lowpass filter and directly couples other IM products to the Diplexer. The lowpass filter removes odd multiples of 2.072 GHz that are re-entrant modes of the Directional Filter. The Diplexer provides dc path for mixer bias and rejects frequencies above 829 MHz.

The single balanced 1st Mixer affords less IM products than an unbalanced mixer, so the conversion loss is inherently less. It also cancels local oscillator signal feed-through to the RF input port.

In standard instruments, an external mixer port and Transfer Switch are included. Option 08 deletes these features. The external mixer feature permits an external mixer to be connected to the instrument to serve as the 1st IF source. This feature is primarily used for waveguide mixers.

For Option 01 instruments, a Preselector or 1.8 GHz lowpass filter is inserted in the RF signal path. The signal passes through a low-band/high-band switch, which selects the Preselector or the 1.8 GHz lowpass filter. The 2 GHz Limiter protects the 1st mixer diodes from signals 2 GHz and above by reflecting RF energy back to the input source. The 1.8 GHz lowpass filter attenuates signals above 1.8 GHz to reduce spurious responses caused by RF signals above 1.8 GHz feeding through to the 1st mixer.

The Preselector is the signal path for frequencies from 1.7 to 21 GHz. The Preselector is a tunable filter that tracks with the 1st local oscillator. This prevents other RF signals from feeding through to the 1st mixer and eliminates spurious responses from external sources. From the Preselector the signal passes through a 3 dB attenuator, which improves the return loss of the Preselector, to the 1st Mixer.

RF INTERFACE CIRCUITS ⟨27⟩

Introduction

Refer to the block diagram adjacent to Diagram 27. The RF Interface circuits receive address and instruction data from the Microcomputer, decode it, and control the RF Attenuator, Transfer Switch, and IF selection. The circuit consists of the Digital control circuits, which decodes the address and control the input data to the buffer. The RF Interface section also includes the driver circuits, which furnish the current required to drive the three functions mentioned at the first of this paragraph.

Digital Control

Address decoder U2045 enables the data at the input of U3046 whenever address 4F is selected by the Microcomputer. Table 5-1 lists the purpose of each data line from the buffer.

Transistors Q2025 and Q3028 are enabled by a negative pulse from the microcomputer. The two transistors raise the Vcc of the three attenuator drivers (U3034, U3029, and U3038) to +16 V for about 100 ms; this furnishes sufficient voltage to energize the attenuator solenoids. Each of the attenuator driver output lines is protected by a diode from the inductive kick that occurs when the solenoids change state.

Transfer Switch

Amplifier U4023, transistors Q3025 and Q3024, plus related components form the driver circuit for the Transfer Switch. To select the external mixer, the microcomputer sets line Q5 high. The change is coupled through C4026 and R4012, which hold U4023 at a low output state for a few milliseconds. This lets Q3025 conduct, and the Transfer Switch selects the external source. If the microcomputer selects the internal mixer, it pulls line Q5 low, switching U4023 in the opposite direction, which causes Q3024 to conduct. The Transfer Switch energizes in the opposite direction, and the internal mixer is part of the circuit. Diodes CR3018 and CR3017 protect the transistors from voltage spikes induced by the Transfer Switch when it changes state.

Timer

M1019 is an electrochemical timer. The current through R1015 causes the copper band to progress along the scale that is calibrated for a duration of 5000 operating hours.

Table 5-1
RF INTERFACE LINES

Line	Purpose
Q1	Enables 10 dB attenuator
Q2	No connection
Q3	Enables 30 dB attenuator
Q4	Enable current drivers Q2025 and Q3028
Q5	Enables transfer switch driver
Q6	Selects 829 MHz IF (high state) or 2072 MHz IF (low)
Q7	Enables 20 dB attenuator
Q8	Enables baseline clipping

RF CIRCUITRY ⟨12⟩

Introduction

Refer to the block diagram adjacent to Diagram 12. The input signal is processed through a calibrated 0—60 dB attenuator (10 dB steps) and applied to the 1st Mixer. Option 01 instruments add a limiter and a 1.8 GHz lowpass filter, or a current-tuned preselector, between the attenuator and the 1st Mixer to improve selectivity. The IF output of the 1st mixer is sent through Transfer Switch S13 to a directional filter where 2.072 GHz and 829 MHz intermediate frequencies are selected for the 2072 MHz 2nd Converter or 829 MHz 2nd Converter. The 2072 MHz IF is fed through a 4.5 GHz lowpass filter (to reject the re-entrant modes of the directional filter) to the 2072 MHz 2nd Converter. The 829 MHz signal is fed through a diplexer and a 4.5 GHz filter before it is applied to the 829 MHz IF stages. The 4.5 GHz filter is used to reject the re-entrant modes of an internal filter to the 829 MHz 2nd Converter. Two intermediate frequencies are used in the analyzer to prevent baseline rise due to local oscillator feedthrough and crossover intermodulation products.

The 2072 MHz IF is selected for bands 1 and 5, plus the waveguide bands. The 829 MHz IF is selcted for bands 2—4. With Option 01 installed, band 1 frequency range is limited to 1.8 GHz, due to a lowpass filter. A tunable preselector is used instead of the lowpass filter when bands 2 through 5 are used. Refer to Diagram 12 while reading the following description.

RF Signal Path

The 0—60 dB step attenuator consists of three sections (10 dB, 20 dB, and 30 dB), which are controlled by relays that receive drive signals from the RF Interface circuit. The output of the attenuator is connected directly to the 1st Mixer through a 3 dB attenuator in analyzers not equipped with Option 01. The attenuator protects the mixer diodes from excessive input voltages and static discharges. In analyzers equipped with Option 01, the Preselector and related circuitry is placed between the step attenuator and the 3 dB attenuator.

1st Mixer

The 1st Mixer receives the RF signal through the 3 dB attenuator, and generates the intermodulation products that are filtered to provide the low and high IF signals. The mixer is a single balanced design, which has less conversion loss in comparison with unbalanced mixers. The local oscillator input is split through a broadband multi-section coupler, whose outputs are equal in power but 90 °s out of phase. An additional 90 ° phase shift is cascaded with the appropriate signal to create a 180 ° phase difference that is applied across a pair of series-connected Schottky diodes. The result is that the diodes are alternately switched on and off as the local oscillator cycles. The node between the two diodes is isolated from the 1st LO input by about 30 dB, so the RF input is applied to this node. The blocking capacitor at the input connector permits broadband signal application from the RF port, while blocking dc diode bias from appearing at the analyzer input. Dc return for the mixer is by way of the Transfer Switch, Directional Filter, Diplexer, and 4.5 GHz filter through the 829 MHz IF circuits. The mixer bias voltages arrive at the mixer through the same path.

Not counting the IF filtering circuitry, the fundamental conversion loss of the 1st Converter is about 14 dB; third harmonic conversion loss is about 24 dB. The Schottky diodes are mounted in a removable assembly that can be extracted or inserted in the main mixer module.

Power Divider

The Power Divider splits the output of the 1st LO (YIG oscillator) to isolate the 1st Mixer from the 1st LO OUTPUT front-panel connector. The unit is essentially two multisection directional couplers that are multi-port cascaded to produce two ports having equal power. The isolation between output ports is greater than 15 dB at operating frequency. The Power Divider also provides an improved load to the local oscillator.

1st Local Oscillator

The 1st LO is a YIG (Yitrium-Iron-Garnet) oscillator that has a tuning range of 2.072 to 6.35 GHz. The oscillator assembly includes the interface circuit board that couples operating and tuning voltages from the 1st LO Driver, Span Attenuator, and Error Amplifier circuits to the oscillator.

The +15V1 voltage provides operating bias for the oscillator. The supply is protected by VR1010, C1016, and R1011. The second supply, +15V2, is for future applications. CR1018 and CR1019 stop transient voltages from entering the tune voltage coils. It also protects the driving circuits from the transients induced when degaussing.

Relay K1015 is closed when the FM Coil is used to tune the oscillator. To prevent the tune volts coil from moving the oscillator frequency while the FM Coil is in operation, C1012 and C1014 are connected across the tune coil. The heater keeps the YIG sphere at a constant temperature for best stability.

Transfer Switch

The Transfer Switch is a three-port coaxial switch that permits application of 1st IF signals from inside or outside the analyzer. This feature is primarily used for by-passing the 1st Converter circuitry. The function is controlled by circuitry on the RF Interface board. It is automatically actuated when waveguide bands are selected, or the front-panel EXT MIXER push button is pressed.

Directional Filter

The Directional Filter (FL16) couples the 2072 MHz signal to the 2nd Converter via the lowpass and bandpass filters. As intermodulation products (IM) flow through FL16, they induce a selected current into a one-wavelength distributed ring, which couples the 2072 MHz IF signal out to FL11, the lowpass filter. The remainder of the IM products pass on through, since the ring is excited only with 2072 MHz signals. The bandwidth of this unit is approximately 45 MHz. The unfiltered signals are passed on to the Diplexer.

High IF Filters

The 2072 MHz signal from the Directional Filter is passed through FL11, a lowpass filter that rejects all signals above 4.5 MHz. The second filter, FL14, rejects intermodulation products both above and below 2072 MHz.

Diplexer and Filter

The Diplexer filters the 829 MHz IF signal from the mixer output and sends it to the 2nd Converter through FL15. The Diplexer also provides a good match to the 1st Mixer IF port at frequencies above 1 GHz. This match is important for the overall flatness and frequency response of the analyzer.

Preselector

The Preselector, which is included when Option 01 is installed, consists of two selector switches, a 2 GHz limiter, a 1.8 GHz lowpass filter, a 1.7—18 GHz filter, and a 3 dB attenuator.

Coaxial relays S10 and S11 switch the stage input and output to select either the lowpass filter and Limiter or the Preselector and 3 dB attenuator. The relay coils are driven by circuitry on the Preselector Driver board. The lowpass filter path is used only on band 1; the Preselector operates on all the other bands.

The 2 GHz Limiter operates from 100 kHz to 2 GHz. It has a linear two-port transfer characteristic of unity (minus 1 dB) until the input exceeds +5 dBm. Above this point, the internal detector diodes conduct, reflecting part of the RF input energy back to the source. As the input level rises, the limiter reflects more signal, thus limiting the amount that can pass through.

The 1.8 GHz lowpass filter strips the incoming signal of any frequencies above 1.8 GHz and passes the signal below 1.8 GHz on to the output segment of the selector switch (S11).

The Preselector is a 1.7—18 GHz YIG Filter that provides high selectivity and image-frequency rejection. Tuning current, which is near 500 mA at 21 GHz, is provided by the Preselector Driver circuits. The Preselector operates on bands 2, 3, 4, and 5. The signal from the Preselector passes through a 3 dB attenuator to the output section of the Filter Selector switch. The attenuator isolates the Preselector, which is sensitive to loading on its output.

2ND CONVERTER CIRCUITS

Two 2nd Converter systems are used in the 492/492P Spectrum Analyzer. One converts 2072 MHz to 110 MHz; the other converts 829 MHz to 110 MHz. Only one converter is operational at any time, and is selected as a function of the measurement band being used. The selection of the IF for each band is shown in Table 5-2 along with the center frequency range and the local oscillator frequency range. Note that this table includes Option 01 characteristics.

Two IF's are used by the 2nd Converter for the following reasons:

1) to eliminate IF feedthrough in band 2 and reduce or eliminate higher order spurs in bands 3 and 4;

2) because of the limited tune range of the 719 MHz LO, the lower IF cannot be used above band 4;

3) if a measurement band were to include the first intermediate frequency within its range, it is possible for some input signals admitted by the preselector to pass through the 1st Converter (without conversion), into the 2nd converter at the 1st intermediate frequency. The resultant spurious output will cause the baseline level on the screen to rise, and could possibly obscure real signals. By using two selectable 2nd Converters, the analyzer can have overlapping measurement bands that do not include the first intermediate frequency, and completely avoid the problem.

The 2072 MHz 2nd converter mixes the 2072 MHz from the first converter with the output from a cavity oscillator. This local oscillator is swept over a 7.5 MHz range. At the converter input, a four-cavity bandpass filter is used to pass only the 2072 MHz 1st IF signal and prevent unwanted signals generated within the 2nd Converter from passing back through to the 1st Converter. A diode mixer is used to mix the 2072 MHz IF input and the local oscillator signals to generate the 110 MHz second IF output. The 110 MHz output passes through a 110 MHz lowpass filter that blocks higher frequency signals from the mixer.

The 829 MHz 2nd Converter uses a phase-locked voltage controlled oscillator to produce the 719 MHz signal that is mixed with the 829 MHz first IF signal. The swept 2182 MHz 2nd local oscillator is used as a reference for the 719 MHz local oscillator. The 719 MHz oscillator is designed so that it can be disabled upon command from the microcomputer in the IF selection process. The phaselock circuit maintains a constant relationship between the two local oscillators as the 719 MHz oscillator is swept over a 2.5 MHz range. A four-section coaxial bandpass filter is used before the mixer to exclude any RF signals other than the desired 829 MHz first IF. Again, a diode mixer is used to mix the 829 MHz input and local oscillator signals to produce the 110 MHz second IF output.

Selection between the two IF signals also takes place within the 829 MHz converter system. Under command of the microcomputer (by way of the RF Interface circuits) a diode selector switching network connects one of the two 110 MHz second IF signals to the output for application to the 3rd Converter.

Table 5-2
2ND CONVERTER IF SELECTION

Frequency Band	Center Frequency Range	Local Oscillator Frequency (MHz) Range	Converter System IF
1	0—1.8 GHz	2182 ±3.75	2072 MHz
2	1.7—5.5 GHz	719 ±1.25	829 MHz
3	3.0—7.1 GHz	719 ±1.25	829 MHz
4	5.4—18.0 GHz	719 ±1.25	829 MHz
5	15.0—21.0 GHz	2182 ±3.75	2072 MHz
6	18.0—26.5 GHz	2182 ±3.75	2072 MHz
7	26.5—40.0 GHz	2182 ±3.75	2072 MHz
8	40.0—60.0 GHz	2182 ±3.75	2072 MHz
9	60.0—90.0 GHz	2182 ±3.75	2072 MHz
10	90.0—140.0 GHz	2182 ±3.75	2072 MHz
11	140.0—220.0 GHz	2182 ±3.75	2072 MHz

2072 MHz 2ND CONVERTER ⟨13⟩

The 2072 MHz 2nd Converter converts the 2072 MHz signal output from the 1st Converter to 110 MHz for eventual application to the 3rd Converter. The assembly consists of a low-loss narrow-band four-cavity filter connected through an internal cable to a low conversion loss narrow-band diode mixer, a 110 MHz lowpass filter, and a mixer biasing circuit that will disable the mixer when directed by the microcomputer.

Four-Cavity Filter

The Four-Cavity (bandpass) Filter, which is depicted on Diagrams 11, 12, and 13, is designed to pass only the 2072 MHz IF signal to the mixer and to reflect any other frequencies back to the 1st Converter for termination. In addition, the filter keeps the converter LO and mixer products from entering the 1st Converter.

This filter is designed for a 1 dB bandwidth of 15 MHz and an insertion loss of 1.2 dB. Each end resonator is capacity coupled to external circuits through a coupling hat plugged into a 3 millimeter connector. Intercavity coupling is provided by coupling loops that protrude from the machined filter top. The resonant frequency of each cavity is determined primarily by the depth of a gap in the underside of the

filter top, and is fine tuned with a tuning screw on the side of each cavity. All of the tight machining tolerances are confined to the top. Thus, the main cavity milling need not be a high precision part. When properly tuned, using a network analyzer, the filter return loss is greater than 25 dB from either end (in a 50 Ω system). Figure 5-1 shows a cross sectional view of the filter; Fig. 5-2 shows the equivalent electrical circuit.

Mixer Circuit

The Mixer circuit in the 2072 MHz 2nd Converter is of the single-balanced, two-diode type, and consists of the mixer, an operational amplifier bias circuit, a delay line, and a lowpass filter. In opertion, both diodes of the mixer are turned on and off by the output signal from the 2181 MHz 2nd Local Oscillator, through coaxial connector P183. Note that, although the diodes are connected for opposite polarity, both are turned on at the same time because of the 180° phase shift delay line in the input line to the upper deck. Also note that the diodes are matched and must both be replaced if one fails.

2072 MHz RF from the Four-Cavity Filter enters the mixer, where it is switched on and off at a 2182 MHz rate by the mixer diodes. Conduction of the diodes is controlled by the much stronger 2181 MHz LO signal. Several mixing products result; one, the difference frequency of 110 MHz, is separated from the others by a low-pass filter for use as the IF output.
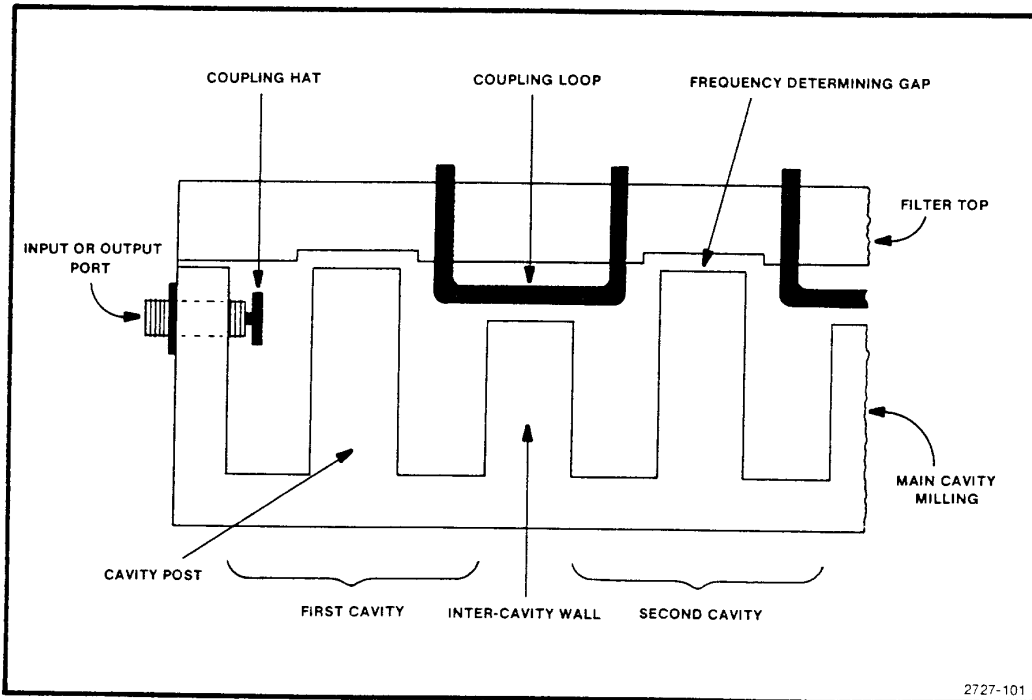

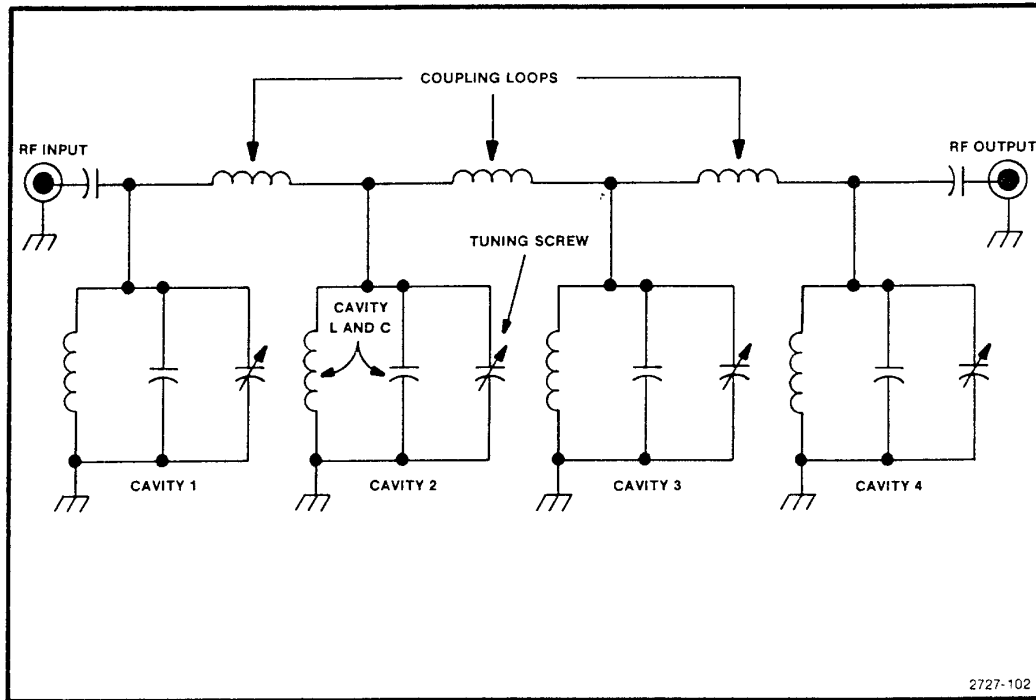
Fig. 5-1. Filter cross-section view.

Fig. 5-2. Filter equivalent circuit.

The two inductors and one capacitor at the output of the mixer form a lowpass filter that passes 110 MHz unattenuated to the 829 MHz 2nd Converter via coaxial connector P182. Capacitors at each of the three inputs to the mixer function as dc blocking capacitors to keep the diode bias from being impressed upon the RF and local oscillator lines.

The bias circuit, which consists of operational amplifier U1014 and the associated components, establishes the bias for the mixer diodes and also provides the means for effectively switching the mixer off (under control of the microcomputer). When the mixer is active, each diode has approximately 2 mA of forward bias. For this condition, the IF SELECT signal from the Z Axis/RF Interface circuits (applied through feedthrough capacitor C182) is low. This causes the output from U1014A to be at +14 V and the output from U1014B to be −14 V. Diodes CR1014 and CR1018 are thereby reverse-biased. Thus, the series resistances of potentiometer R1019 and resistor R1014, and potentiometer R1010 and resistor R1017 provide forward bias to the diodes. The potentiometers provide for balancing the bias levels.

In operations in which the mixer is not active, the IF SELECT signal is high. This reverses the states of the U1014 outputs and forward-biases diodes CR1014 and CR1018.

With these diodes conducting, resistors R1014, R1016, R1017, and R1018 form two voltage dividers that set the reverse bias to the mixer diodes at 5 V. This effectively turns the mixer off, and attenuates the 110 MHz signal by about 55 dB.

Precision External Cables

The external cable that connects the Four-Cavity Filter output to the mixer circuit and the external cable that connects the cavity 2nd Local Oscillator to the mixer circuit are both critical length cables. The reasons the length is critical are as follows:

The 4-Cavity Filter-to-Mixer input cable: Several products and harmonics of the local oscillator and RF input frequencies are allowed to exit the mixer via the RF input port of the mixer. Two significant products are the image (RF input minus the 2nd Local Oscillator) and the sum (RF input plus the 2nd Local Oscillator). There is enough energy in these two signals to warrant efforts to recover that energy.

Only the RF signal at 2072 MHz can pass through the Four-Cavity Filter. Thus, any other frequency applied to the

filter (that is, signals exiting the mixer via the RF port) is reflected back to the mixer by the filter. If the cable between the filter and the mixer is the correct length, the most significant reflected signals (that is, the image and the sum) can be returned to the mixer in phase and converted into additional energy at the intermediate frequency. This technique is called "image enhancement mixing" and typically improves conversion loss by approximately 3 dB at the design frequencies.

The image frequency in this instance is very near the RF frequency. A very sharp cut-off filter is thus required to pass the RF, yet reflect the image. The Four-Cavity Filter performs this function.

The 2nd Local Oscillator-to-Mixer LO input cable: The image and sum products are also present at the LO port of the mixer. These signals leave the mixer via the cable to the 2nd LO and are reflected back to the mixer by the LO. The oscillators resonator appears highly reflective to the image and sum signals because it is tuned to the LO frequency. Again, the length of the cable from the LO to the mixer LO port is adjusted so the image and sum signals are reflected back to the mixer in the proper phase for re-conversion to supply additional energy at the IF frequency.

2182 MHz PHASELOCKED 2ND LO

⟨38⟩A & ⟨38⟩B

General Description

The 2182 MHz Phaselocked 2nd LO assembly contains a tunable microwave oscillator, frequency reference circuitry, and phaselock circuitry, within a two-section housing. Microwave circuitry is packaged within the machined aluminum portion of the housing. Low frequency phaselock circuitry is within the mu-metal compartment.

In the microwave or LO portion of the assembly, the 2182 MHz Microstrip Oscillator generates 2182 MHz for the 2nd converters and the 2nd LO internal reference circuitry. The 2200 MHz Reference circuit receives a 100 MHz drive signal from the 3rd converter crystal oscillator and produces 100 MHz harmonics. The 22nd harmonic or 2200 MHz is mixed with 2182 MHz from the microstrip oscillator in the 2200 MHz Reference Mixer circuit. The difference frequency of 18 MHz is then fed to the phaselock side of the module.

A phase/frequency detector, on the 14-22 MHz Phaselock circuit board, compares the 18 MHz difference frequency with a signal from a linearized tuning 18 MHz voltage controlled oscillator. The detector output tunes the

2182 MHz Microstrip Oscillator such that the difference frequency exactly matches the frequency of the 18 MHz reference VCO.

Sweep and tune signals from the Span attenuator and Center Frequency Control circuits tune the 18 MHz VCO. The output voltage from the phase/frequency detector forces the Microstrip Oscillator to tune the same amount.

2182 MHz MICROSTRIP OSCILLATOR

⟨38⟩B

This oscillator consists of a printed 1/2 wavelength resonator driven by a common-emitter feedback amplifier (Q1021). The base of Q1021 is capacitively tapped into the resonator. The resonator serves as a tuned phase inverter and impedance transformer, connected between the base and collector of Q1021. Part of the base feedback capacitance is provided by a bendable tab (C1021). This allows fine adjustment of the total feedback. This feedback RF signal is detected, by the base-emitter junction of Q1021, to produce a change in bias voltage that is related to the amount of feedback. The base voltage can be monitored at TP1015 with a high impedance voltmeter without significantly disturbing the oscillator.

The dc collector voltage and current for Q1021 is regulated by an active feedback circuit containing transistor Q2021. Voltage at the junction of R2023 and L2023 is a function of Q1021 collector current. This voltage is sensed by Q2021, which alters the base current to Q1021 thereby regulating the collector current and maintaining +10 V dc on the resonator. Decoupling and control of bias loop dynamics are provided by C2104. Resistor R2016 swamps the negative base resistance of Q1021 to provide stabilization. Resistor R2015 protects the base-emitter junction of Q1021 from excessive reverse bias in the event the +12 volt supply fails.

The oscillator is tuned by varactor diode CR1028, connected to one end of the resonator. Decoupling for the varactor is provided by the low-pass elements in the tune line. Bendable tab C1022 can be used to fine tune the oscillator center frequency.

Three output taps are coupled to the resonator through printed capacitors under the resonator. One output supplies 2182 MHz through a 6 dB attenuator to the Harmonic Mixer in the 829 MHz 2nd Converter. The other two output taps couple LO power through 6 dB attenuators to buffer amplifiers Q1031 and Q1011. The amplifiers provide approximately +10 dBm to the 2072 MHz 2nd Converter and +8 dBm to the Reference Mixer.

Since the two buffers are nearly identical, only the 2nd Converter buffer is described. Gain is provided by a single common-emitter transistor (Q1011). Printed elements provide input and output impedance matching. Out-of-band damping is provided by R1011 in series with a 1/4 wavelength shorted stub. Dc is blocked by C1014 and C1011. A 1/4 wavelength open stub is used at the output to reflect one of the 2nd Converter's image frequencies at 4254 MHz (the other buffer does not use nor need this stub). Collector bias for Q1011 is provided through R1012, L1011, the 1/4 wavelength shorted stub, and R1011. The 1/4 wavelength shorted stub is grounded through C2011 (C2011, C1013, and L1011 are also used for decoupling). Collector voltage is determined by divider R1013 and R2013; this controls the dc feedback to the collector-base junction of Q1011. The bias network is decoupled from the RF path by L1014. Diode CR2013 protects the base of Q1011 from excessive reverse bias if the +12 volt supply fails.

2200 MHz Reference Board ⟨38⟩B

This circuit generates harmonics of the 100 MHz input. The 22nd harmonic or 2200 MHz is used by the Reference Mixer. The input 100 MHz signal is applied through a matching network (consisting of L1034, L1025, C1036, C1029, and C1025) to a differential amplifier (Q1024 and Q2024). The emitters of this amplifier are ac coupled through C2026, reducing low frequency gain and ensuring balanced operation. A snap-off diode (CR2014) is driven by the amplifier, via transformer T2015, to generate multiple harmonics of the 100 MHz signal including the 2200 MHz reference. The output passes through a 3 dB attenuator, for isolation, to the Reference Mixer circuit.

2200 MHz Reference Mixer ⟨38⟩B

Signals from the 2200 MHz Reference circuit are filtered by a printed 2200 MHz bandpass filter. Diodes CR1011 and CR1012 are the switching elements of a single-balanced mixer. The microstrip oscillator output is applied to CR1011 and through a 1/2 wavelength delay line to CR1012. The delay line shifts the oscillator signal 180° so both diodes switch together. Mixing the 2200 MHz with the oscillator 2182 MHz signal produces the difference frequency of 18 MHz. This 18 MHz signal is fed through a 37 MHz lowpass filter to the 14-22 MHz phaselock circuit. The lowpass filter prevents unwanted products, such as 82 MHz (product of 2100 MHz and 2182 MHz), from passing into the phaselock circuit.

14-22 MHz Phaselock Board ⟨38⟩A

This board contains regulated power supplies, a 14-22 MHz (18 MHz nominal) voltage controlled oscillator with linearizing circuitry, and a phase/frequency detector circuit.

Its main function is control of the 2182 MHz Microstrip Oscillator. The entire circuit board is housed in a magnetic shield to reduce spurious effects of external ac fields. All power supply and control inputs enter the circuit board via feedthrough capacitors in the housing wall. All connections with the microwave circuitry are through feedthrough capacitors C2200-C2204, in the floor of the housing.

The +15 V, −15 V, and +9 V inputs supply power to operational amplifier type regulators that produce +12 V, −12 V, and +5.2 V outputs, respectively. A zener diode (VR2021) serves as a stable −6.2 V reference for U2014B, which regulates the −12 V supply through emitter-follower Q2021. The −12 V supply, in turn, provides bias current for VR2021. Diodes CR2015 and CR2018 protect the operational amplifier output and Q2021 during supply shutdown. Inverting amplifiers U2014A/Q1012 and U1015/Q1022 use the −12 V supply as a reference to produce the +12 V and +5.2 V supplies, respectively.

The 2nd LO sweep and tune inputs are summed by differential amplifier U2063. Ground potential of the Span Attenuator circuit is sensed through R2057 and subtracted from the sweep signal to reduce effects of ground potential variations. Provision is made for sensing the ground potential of the Center Frequency Control circuit board through R2059; however, the present interface requires that the Fine Tune ground input be grounded to the 2nd LO assembly through W2059. Sweep and tune sensitivities are set by selectable resistor R2063.

The combined sweep and tune signals, at the output of U2063, are applied to a non-linear shaping circuit, the gain of which varies as a function of input signal voltage. Output voltage from the shaper circuit controls the bias of varactor diode CR1075. This bias tunes the 14-22 MHz oscillator. Non-linear tuning characteristics of the oscillator are compensated by reciprocal non-linearity in the shaper. As the input voltage to non-inverting amplifier U1062B becomes more positive, it successively exceeds the tap-point voltages of a series of positive voltage dividers. Diodes in U2051, connected to the divider tap points, are successively forward biased to add increasing shunt conductance to the amplifier's feedback path. Feedback progressively decreases and forward gain of the amplifier increases with positive excursions. A similar amplifier, U1062A, uses negative voltage dividers and the diodes in U1051 to increase the gain progressively with negative voltage excursions. Outputs of the two amplifiers are summed at R1068, which is selected to match the gain shaping requirements of the 14-22 MHz oscillator. One of the varactor bias resistors, R1070, is also selected as part of the linearity adjustment.

The 14-22 MHz oscillator consists of a differential amplifier with transformer feedback. The emitters of the amplifier transistors Q2073 and Q2078 are ac coupled through

C2077. Transformer T1077 serves as the amplifier feedback path and also as part of the oscillator resonator. Tuning varactor CR1075 provides virtually all of the resonator capacitance to allow a wide tuning range. Transformers T1077 and T1075 constitute the resonator inductance that may be selected by using different tap combinations to interconnect the two coils. Resonator inductance is adjusted to center the oscillator's tune range near 18 MHz. R2076 and R2079 enhance the amplifier high frequency stability.

A discrete two-stage amplifier provides an unsaturated voltage gain of approximately 43 dB for the difference frequency signal from the 2200 MHz Reference Mixer. The output of Q1036 drives a differential amplifier consisting of Q1037 and Q1038. The differential stage limits the output swing to ECL compatible levels. Dc bias for the amplifier is provided by Q1036, which has dc collector-base feedback via voltage divider R1039 and R1041. ECL line receivers U2036D and U2036B buffer signals from the discrete amplifier and the 14-22 MHz oscillator, respectively. Output signals from these amplifiers are applied to the phase/frequency detector for comparison.

A pair of ECL D-type flip-flops (U2027A, U2027B) comprise the phase/frequency detector. The flip-flop outputs are wired and connected to the input of U2036C, which serves as a common reset. The clock input to U2027B is the 14-22 MHz VCO signal, and the clock input to U2027A is the amplified difference signal from the Reference Mixer. If the two clock signals are of identical phase and frequency, both flip-flop sections set then reset together. If the phase of the Reference Mixer signal leads the 14-22 MHz signal, U2027A will remain set longer than U2027B. If the signal lags, U2027B will set first and remain set longer. The signal that leads in phase or has the higher frequency will cause the associated flip-flop to remain set a higher percentage of the time. The average differential output voltage of the two flip-flops therefore indicates whether the Reference Mixer signal leads, lags, or differs in frequency from the 14-22 MHz VCO reference. Output of the detector is filtered by an RC lowpass filter, then applied to differential amplifier U1028, which tunes the 2182 MHz oscillator.

The phaselock circuit adjusts the Microstrip Oscillator frequency such that the Reference Mixer output always matches the frequency of the 14-22 MHz VCO. The Microstrip Oscillator is therefore locked to a frequency equal to that of the 2200 MHz reference minus that of the 14-22 MHz VCO. If the 14-22 MHz Oscillator is swept or tuned, the Microstrip Oscillator sweeps and tunes an equal amount. Within the control bandwidth of the lock loop, the Microstrip Oscillator FM noise is reduced to that of the reference circuitry. The phaselock loop bandwidth is controlled by R1024, C1026, and R1025, C1023. Unity gain for the phaselock loop occurs near 200 kHz with a gain slope of −6 dB/octave. The gain slope breaks to −12 dB/octave for frequencies below 16 kHz. Resistors R1030 and R1031 di-

vide and offset the output of U1028 so the Microstrip oscillator tune voltage ranges between 0 and −12.5 V.

CAVITY 2ND LOCAL OSCILLATOR ⟨38⟩

Refer to the block diagram adjacent to Diagram 38. The Cavity 2nd Local Oscillator generates the 2182 MHz signal that is:

1) mixed with the 2072 MHz signal from the 1st Converter to produce the 110 MHz intermediate frequency in the 2072 MHz 2nd Converter; and

2) used as a reference in the harmonic mixer in the phase lock circuit of the 829 MHz 2nd Converter.

The oscillator is a low noise cavity oscillator that free-runs at a nominal frequency of 2182 MHz, but is tunable over a range of 8 MHz. A relatively large resonant cavity with very high Q allows the oscillator to operate at low noise levels and with a power output of +10 dBm. The cavity itself operates in the TEM mode and utilizes a foreshortened vertical post to form a coaxial structure.

Two equivalent schematic diagrams are shown in Fig. 5-3, a direct connection representation, and the RF equivalent.

As shown in the RF equivalent diagram, transistor Q1 operates as a common emitter oscillator with positive feedback in the collector circuit. It is biased to operate with an emitter current of approximately 30 mA. The collector is coupled to the tunable resonant cavity by a coupling screw. Line length between the transistor collector and the coupling screw is set by an adjustable wire strap.

Energy distribution inside the cavity is such that E fields are at the top of the cavity and magnetic (H) fields circulate at the bottom. Energy is extracted from the tank circuit (cavity) by inductive coupling near the bottom of the cavity. The output connectors, with attached coupling loops, are rotated to adjust the power output level from the oscillator. One connector is adjusted to provide +10 dBm of output, and the other is set to provide 0 dBm of output power.

Tuning of the oscillator frequency is by means of a varactor diode that is controlled by a 15 to 40 V bias signal from the Shaper and Bias circuit. This signal varies the oscillator frequency over an 8 MHz range. The diode is located near the top of the cavity and is coupled to the cavity post by a capacitive coupling hat (E-field coupling). RF energy in the coupling hat is decoupled from the varactor bias feedthrough by an inductor. The spacing between the hat and the post determines the sensitivity for the diode tuning.

(This is an adjustment that is performed during manufacture. No attempt should be made to readjust spacing because diode package cracking may occur.)

DIRECT CONNECTION EQUIVALENT
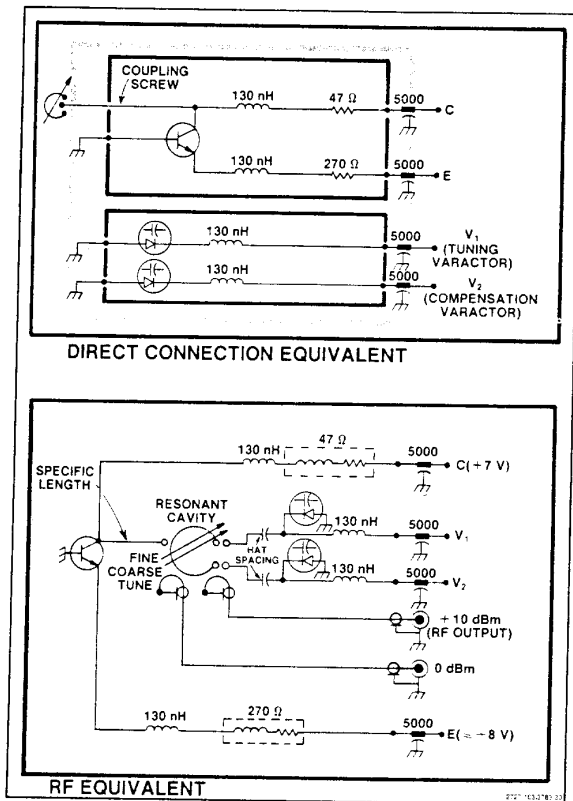

RF EQUIVALENT

Fig. 5-3. 2182.0 MHz Cavity LO equivalent circuits.

A tuning screw is added to the cavity to allow frequency adjustment of the oscillator without removing the LO from the instrument. Figure 5-3A shows the two cavity 2nd LO equivalent circuits.

829 MHz 2ND CONVERTER ⟨15⟩

IF Section

Refer to the block diagram adjacent to Diagram 15. The 829 MHz 2nd Converter converts the 829 MHz signal output from the 1st Converter to 110 MHz for application to the 3rd Converter, and provides the switching capability for the microcomputer controlled selection of either the 2072 or the 829 MHz converter system. The converter circuits consist basically of an input diplexer, an amplifier, a bandpass filter, a mixer, and a diode switch.

829 MHz Diplexer Circuit

The Diplexer passes signals at 829 MHz with minimum attenuation (approximately 1 dB) and has a pass-band of approximately 200 MHz. All frequencies outside the pass-band, from approximately 50 kHz to 2 GHz, are terminated in 50 Ω loads with a match of at least 10 dB. Figure 5-4 shows a simplified schematic of the diplexer.

At 829 MHz, the series resonators provide a low-impedance path from input to output. (Note on Diagram 15 that the input is from the 1st Converter through coaxial connector P231.) Ideally, none of the signal is lost in the 50 Ω resistors because there is a zero impedance path around those resistors. The parallel resonator appears as an open circuit at 829 MHz.

At frequencies above or below the pass-band, the series resonators appear as large reactances, shifting the primary signal flow through the 50 Ω resistors. Also, the out-of-band impedance of the parallel resonator is small compared to 50 Ω. Thus, the resistors are essentially grounded at one end, terminating both the input and output ports. A wide bandwidth is used to minimize losses in the resonators and to eliminate adjustments. Relative bandwidths of the series and parallel resonators are optimized to provide reasonable match at the band edges.

As shown in Diagram 15, the diplexer contains components not shown in Fig. 5-4. Two pairs of 100 Ω resistors (R1012, R1015 and R1011/R1012) are used in parallel to form each 50 Ω termination. This reduces load inductance. A small capacitor is connected across each load (C1010 and C1013) to improve impedance match at frequencies above the pass-band. The inductor in the parallel resonator is a printed length of transmission line that is tapped to establish the correct bandwidth. One end of this inductor is grounded through four capacitors (C1017, C1016, C1019, and C1018) so that dc bias from the 1st Local Oscillator Driver can be introduced to the mixer through the diplexer. Four capacitors are used in parallel to minimize inductance variations and circuit Q degradation. A lowpass filter is included in the bias line to keep noise from the 1st converter.

The diplexer is followed in the signal path by a printed circuit five-element lowpass filter that consists of three shunt capacitors and two series inductors. Cutoff frequency of this filter is approximately 1.2 GHz.

829 MHz Amplifier Circuit

The 820 MHz Amplifier provides approximately 18 dB of signal gain at 829 MHz and consists of two nearly identical amplifier stages in cascade (Q1017 and Q1025), plus a 3 dB
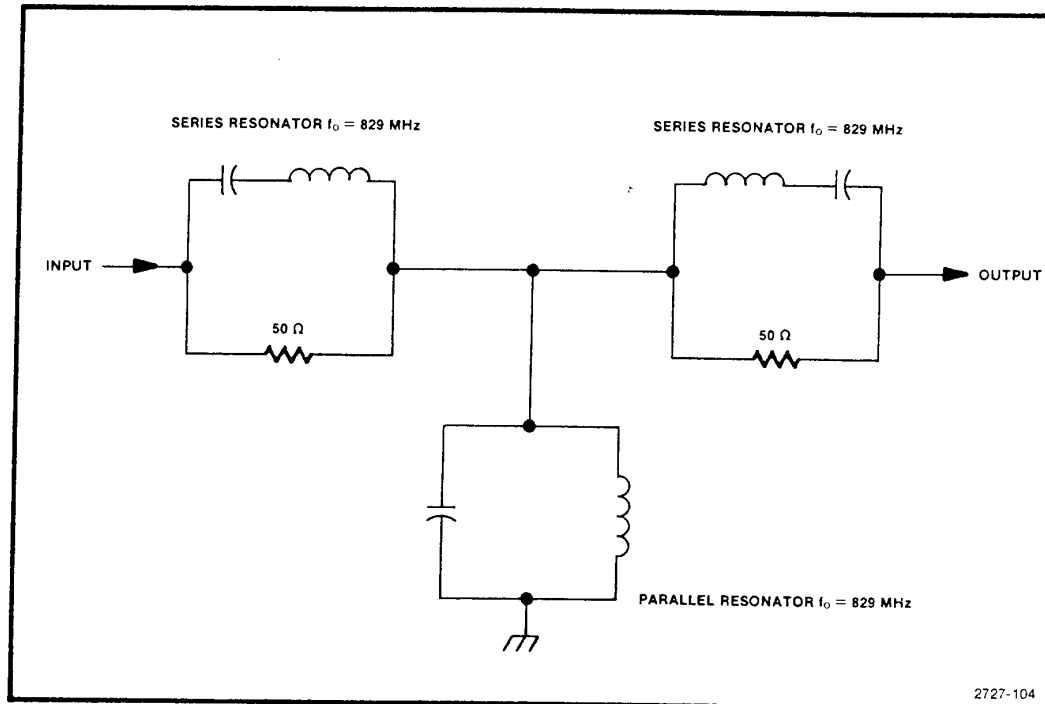
Fig. 5-4. Diplexer simplified schematic.

attenuator. The overall noise figure is approximately 2.8 dB. The gain stages are designed as general purpose, unconditionally stable amplifiers for use in a 50 Ω system. Operation of a stage can be most easily understood if the ac and dc signal paths are described separately. Refer to Figs. 5-5 and 5-6 for simplified schematic diagrams of the ac and dc signal paths.

In the ac circuit of Fig. 5-5, capacitor C1 and printed circuit inductors L1 and L2 form the input matching network. (In the first stage, inductor L1 is actually the series inductance of dc blocking capacitor C1016.) The collector circuit is matched to 50 Ω by inductor L4 and capacitor C2. Gain is controlled primarily by printed circuit emitter inductor L3. High frequency stability is enhanced by resistors R1 and R2. That is, at frequencies well above 829 MHz, resistor R1 ensures low common base gain and resistor R2 helps to dampen the collector circuit.

In the dc circuit of Fig. 5-6, negative feedback through the voltage divider consisting of resistors R3 and R4 sets the collector voltage as a fixed proportion of the −12 volt reference supply. Collector current is determined by resistor R5. Less current is used in the first stage than in the second because the first stage requires less intermodulation distortion performance. Reverse breakdown of the base-emitter junction can degrade the transistor performance, so a diode base clamp is provided in each circuit (CR1013 and

CR1022) for protection in the absence of the +12 volt supply.

Not shown in Figs. 5-5 and 5-6 are an inductor and a capacitor in the base circuits (L1014 and C1014 for Q1017; L1021 and C1023 for Q1025) and a capacitor in the collector circuits (C1013 for Q1017; C1027 for Q1025). These components perform decoupling functions to isolate the signal path from the bias network.

The 3 dB attenuator assists in maintaining a wideband 50 Ω interface between the second amplifier stage and the 829 MHz bandpass filter. It consists of resistors R1026, R1027, R1025, and R1029. A test point (J1029) at the output of the attenuator is used to verify amplifier performance and to aid in adjustment of the following 829 MHz bandpass filter. From the atteunator, the signal is applied to the 829 MHz 2nd Converter Mixer circuit.

829 MHz Mixer Circuits

Refer to Diagram 15. Frequency conversion from 829 MHz to 110 MHz occurs on the 829 MHz 2nd Converter board. The board contains a coaxial bandpass filter, a 1.3 GHz lowpass filter, a 3 dB attenuator, and a two-diode, single-balanced mixer with associated frequency diplexing circuitry.
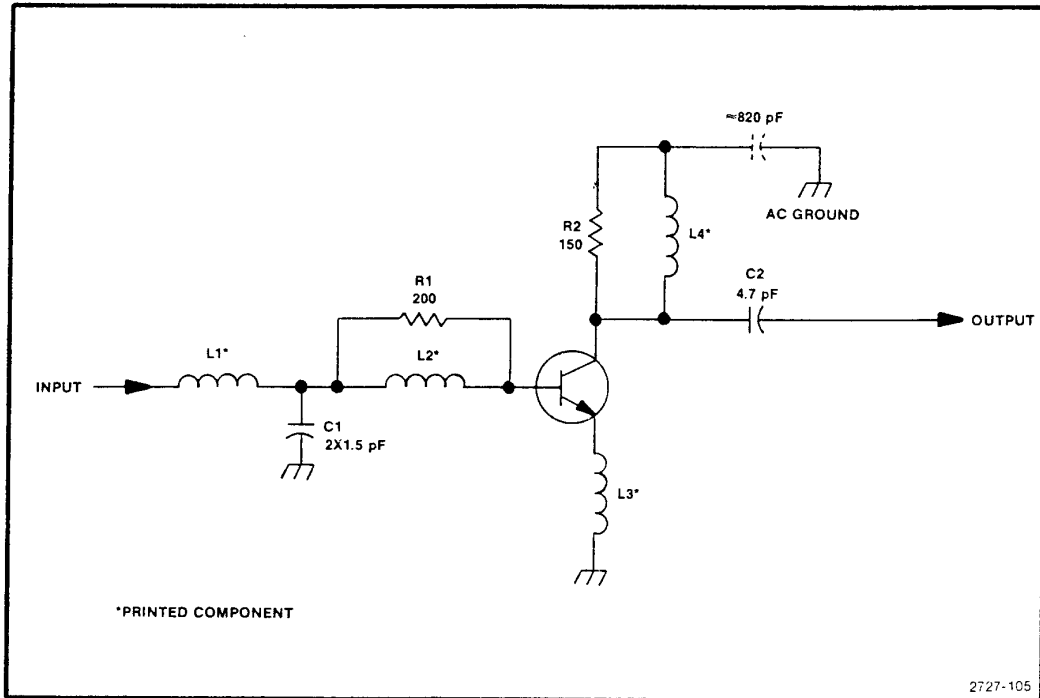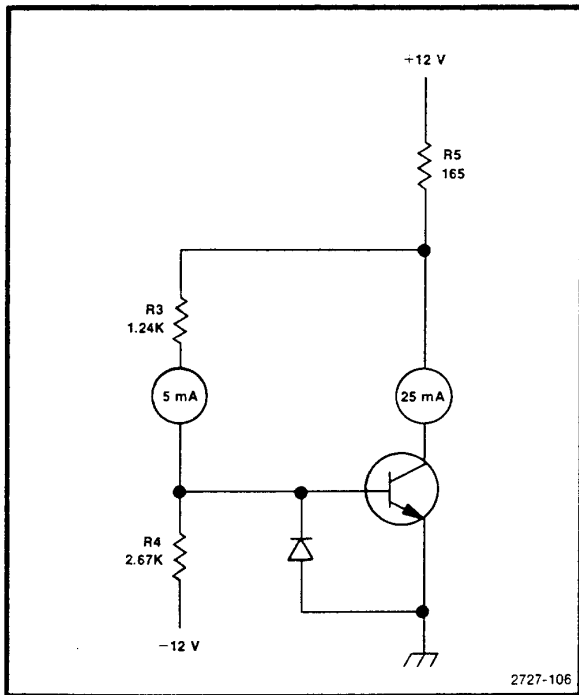
Fig. 5-5. Amplifier signal path.

Fig. 5-6. Amplifier signal path.

829 MHz 1st IF signals from the 829 MHz Amplifier, enters the converter through an 829 MHz bandpass filter. The filter blocks unwanted inputs, primarily the 609 MHz image signal. A 1.3 GHz printed element lowpass filter blocks high frequency signals that would otherwise be admitted at the re-entrant frequencies of the bandpass in excess of 2 GHz. The function of the 1.3 GHz lowpass filter is shared by the 1.2 GHz lowpass filter located on the 829 MHz Diplexer board. A 3 dB attenuator on the 829 MHz Amplifier board and one following the 1.3 GHz lowpass filter help ensure consistent 50 Ω interfaces for the 829 MHz bandpass filter.

The 829 Mhz bandpass filter is composed of four quarter-wave, coaxial-type resonators mounted on the 829 MHz 2nd Converter board. The end resonators are tapped near their grounded end to facilitate the filter's input and output coupling. Inter-resonator coupling is provided by printed "through-the-board" capacitors that connect between the resonators at their high-impedance end. A bendable tab is located at the high-impedance end of each resonator for fine adjustment of resonant frequency. The bendable tab acts as a small, variable capacitance from the end of the resonator to ground, making fine adjustments of resonant frequency possible. When properly tuned, the filter presents an input return loss of at least 12 dB at 829 MHz and an insertion loss of about 2 dB.

829 MHz enters the mixer diodes through a 450 MHz highpass filter. The lowpass filter blocks the lower IF signals generated within the mixer. The mixer diodes are transformer-driven with 719 MHz local oscillator. The large amplitude LO signal (+12 dBm) drives the diodes into and out of conduction, effectively switching the smaller 829 MHz signal on and off at a 719 MHz rate. Several mixing products result, the largest of which are the difference frequencies, (110 MHz) and the sum (1548 MHz). The 110 MHz product is allowed to leave the mixer by way of a 300 MHz lowpass filter that blocks LO, RF, and higher frequency products. The 1548 MHz product leaves the mixer via the 450 MHz lowpass beyond which it is reflected by the 829 MHz bandpass filter and returned to the mixer in-phase with LO harmonics to increase energy of the 110 MHz signal. A printed delay line between the 829 MHz bandpass and 1.3 GHz lowpass filters control the phase delay. The net result of this "image enhancement" is low conversion loss and good inter-modulation distortion performance. Inclusion of the 3 dB attenuator reduces the image enhancement effect considerably but allows line lengths and filter characteristics to be non-critical. Overall conversion loss from 829 MHz to 110 MHz is about 8.5 dB, including 2 dB from the 829 MHz bandpass filter and 3 dB from the attenuator.

110 MHz IF Select Circuits

The 110 MHz IF Select circuits select the 110 MHz IF signal from either the 829 MHz 2nd Converter or the 2072 MHz 2nd Converter for transmission to the 110 MHz IF Amplifier. The 110 MHz IF signal from the 829 MHz Converter is applied directly to the select switch circuit; the 110 MHz IF signal from the 2072 MHz converter is applied (via coaxial connector P233) through a controlled amplifier to the select switch circuit. The switch circuit diodes are CR2011, CR2012, CR2013, and CR1015.

When the IF SELECT signal input to the 829 MHz 2nd Converter (via feedthrough C236) is low, series diode switch CR2011 turns on, allowing the 110 MHz IF signal, from the 829 MHz 2nd Converter, to be applied to the output port. At the same time, shunt diode switches CR2012, CR2013, and CR1015 turn on. Amplifier Q1011 turns off, thus isolating the output port from spurious 2072 MHz 2nd Converter output signals.

When the IF SELECT signal input is high, amplifier Q1011 is turned on and shunt diode switches CR2012, CR2013, and CR1015 turn off. This allows the 110 MHz IF signal from the 2072 MHz 2nd Converter to be applied to the output port. Series diode switch CR2011 also turns off to prevent signal loss into the inactive 829 MHz 2nd Converter. Isolation for the 829 MHz 2nd Converter is not critical when that converter is inactive, because the 719 MHz local oscillator is also turned off by the IF SELECT signal. This eliminates most spurious outputs. The switch and amplifier logic is summarized in Table 5-3.

As described above, diodes are used as the basic switch elements. When forward biased, with current of several milliamps, the diodes present only a few ohms of series resistance to RF signals. When reverse biased, the diodes present essentially an open circuit. The control signal from switch driver Q2015 is connected in a series path through the four diodes (CR2011, CR2012, CR2013, and CR1015) and inductors L2011, L2013, and L2019 so that Q2015 supplies only a small current to forward bias all four diodes. This same diode bias current is used to turn off amplifier Q1011.

Diodes CR2012 and CR2013 are incorporated into a pi-type matching network consisting of inductors L2011, L2013, and capacitor C2012 so that both switches shunt the signal at moderately high impedance points. In addition, when the switch diodes are turned on, parallel resonance, between inductor L2011 and capacitor C2012, presents virtually an open circuit to signals passed by switch diode CR2011. Switch diode CR2013 is located at the high impedance node created by series resonant inductor L2019 and capacitor C2017. Diode CR1015 directly shunts the output from amplifier Q1011.

Transistor Q1011 operates as a common-emitter amplifier for the 110 MHz IF signal from the 2072 MHz 2nd Converter. Its gain and impedance match are controlled primarily by feedback resistors R1011 and R1012. Resistors R1013 and R1018 attenuate the output by approximately 6 dB for enhanced control of match and stability characteristics. Dc collector current from Q1011 develops a voltage across resistor R1017. Bias control transistor

Table 5-3
SWITCH AND AMPLIFIER SELECTION SUMMARY

IF Select Line	Series Switch	Shunt Switch	Amplifier	110-MHz IF Source
High	On	On	Off	829 MHz 2nd Conv.
Low	Off	Off	On	2072 MHz 2nd Conv.

Q1012 then compares this voltage with the fixed voltage of the divider, consisting of resistors R1015 and R1016. Any variation in the Q1011 collector current is thus sensed by Q1012 and cancelled by a resulting change in the Q1011 base current. Collector current in Q1011 is fixed in this manner at approximately 15 mA.

When control current is drawn through the switching diodes by driver Q2015, a voltage is developed across resistor R1017 that exceeds the control limits of Q1012, effectively removing the base bias from amplifier Q1011 and turning off that transistor. Negative current supplied through resistor R1014 ensures that Q1011 can be turned off by the loss of positive base drive. Diode CR1011 protects the base of Q1011 from excessive reverse bias. Voltage across R1017 is approximately 3.4 V when Q1011 is turned on and approximately 4.4 V when it is turned off. Overall gain for the 110 MHz path is approximately 12.8 dB when the amplifier is turned on.

From the diode switch circuit, the 110 MHz IF signal is transmitted via coaxial connector P232 to the 110 MHz IF Amplifier.

829 MHz, 2nd Converter, LO Section

Refer to the block diagram adjacent to Diagram 14. The 829 MHz 2nd Converter Local Oscillator provides the 719 MHz frequency that is mixed with the 829 MHz IF signal to produce the 110 MHz IF signal that is supplied to the 3rd Converter. (In the following description, the circuits are referred to as the 719 MHz LO.) The 719 MHz LO consists of a phaselock loop, a 719 MHz output circuit, and a 2nd LO front panel output circuit. Refer to Diagram 14 while reading the following description.

Phaselock Circuit

The phaselock circuit receives reference frequency inputs and uses phase/frequency detection techniques to use those signals in controlling the output frequency of the 719 MHz oscillator. The circuit consists of a voltage controlled oscillator (VCO), a phase/frequency detector, a harmonic mixer, and various amplification stages and power splitters. When the 719 MHz LO is enabled, the 2182 MHz Local Oscillator output frequency is used as a swept reference to derive the 719 MHz frequency. The VCO is controlled so that the third harmonic of its output frequency is a constant difference from the 2182 MHz reference. This control is accomplished by the phaselock loop. Refer to Fig. 5-7.

In the phaselock loop, the harmonic mixer generates a frequency that is the difference between the swept 2182 MHz input reference and the third harmonic of the VCO output frequency. Ideally, this difference is 25 MHz. That frequency, in turn, is compared with the 25 MHz that is
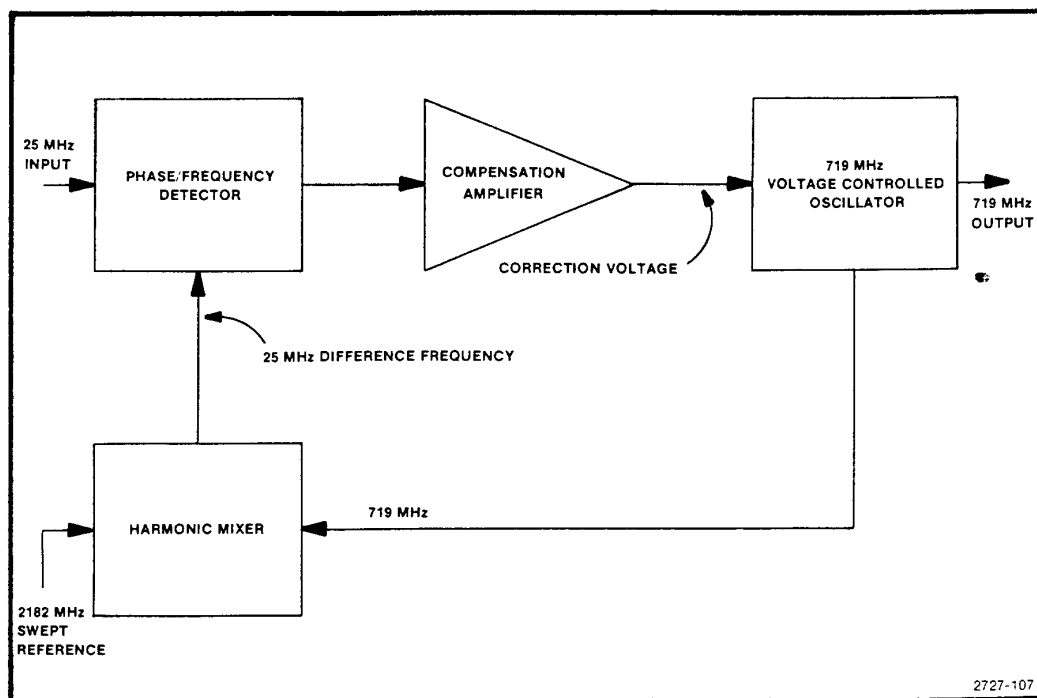

Fig. 5-7. Simplified block diagram of the phaselock circuits.

divided down from the 100 MHz oscillator output supplied from the 3rd Converter. This comparison is done by the phase/frequency detector circuit. Its output is a correction voltage that is applied to the VCO to drive the frequency in the required direction to maintain the nominal output frequency at 719 MHz. This completes the loop that causes the VCO to track the 2182 MHz reference.

Because the third harmonic of 719 MHz oscillator frequency is locked to the 2182 MHz reference, the tuning range of the 719 MHz oscillator is only one third of the swept range of the reference. Since that swept range is 8 MHz, the 719 MHz oscillator range need be only 719 ± 1.33 MHz.

The 719 MHz VCO, Q2014, uses a Colpitts configuration with a printed circuit quarter-wavelength transmission line resonator to achieve high spectral purity and good thermal stability. Correction voltage is applied to varactor diode CR1011 (which is connected at the midpoint of the transmission line resonator) to vary the resonant frequency of the transmission line over a 2.66 MHz range. A tunable transmission line (also printed) adjacent to the printed resonator compensates for variations in component tolerances and resonator dimensions. This adjustable transmission line is cut at factory calibration to the correct length for proper VCO operation. A scale with minor divisions every 2 MHz is printed next to the adjustable line to aid in calibration. The output from the oscillator is extracted near one end of the quarter-wavelength line through two printed inductors and applied to output amplifiers through a power splitter.

Note that the 719 MHz VCO is enabled or disabled under microprocessor control, dependent upon the frequency band being analyzed. When the oscillator is disabled, the 719 MHz signal is no longer available for conversions with 829 MHz RF. This is controlled by the IF SELECT signal from the RF Interface through connector C231. If this signal is low, transistor Q2017 is cut off, which cuts off transistor Q2016. This, in turn, cuts off transistor Q3015 (which is the current source for oscillator transistor Q2014), thus cutting off the 719 MHz oscillator.

From the oscillator, the +6 dBm 719 MHz output signal is applied to isolation amplifier Q1021 through a power divider that consists of resistors R1021, R1022, and R1020. (From the other side of this power divider, the signal is applied to an output amplifier for transmission to the 829 MHz 2nd Converter Mixer circuit.) A second isolation amplifier (Q3021) identical in configuration, provides the necessary isolation between the 719 MHz oscillator output and undesired harmonic mixer products.

The harmonic mixer produces not only the required 25 MHz difference frequency, but also many other higher order products. Two in particular, those at 744 MHz and 694 MHz, are separated from the 719 MHz oscillator frequency by only 25 MHz. Were it not for the isolation provided by amplifiers Q1021 and Q3021, these two products could be converted in the 829 MHz mixer and would thus appear as real signals on the screen. The isolation amplifiers provide sufficient attenuation in the reverse direction to prevent this occurrence.

To provide maximum reverse attenuation in each amplifier circuit, external RF feedback is kept to a minimum. An output matching LC network, consisting of capacitor C1025 and a printed inductor for Q1021, and capacitor C3021 and a printed inductor for Q3021, presents an optimum load impedance to the collector of each transistor to allow maximum power transfer to the attenuator that precedes the harmonic mixer. An input LC matching network consisting of capacitors C1023 and C1022, plus a printed inductor for Q1021 and capacitors C3023, C3022 plus a printed inductor for Q3021, establishes the 50 Ω input impedance to each transistor.

A 3 dB attenuator consisting of resistors R3021, R3022, R2021, and R3023 at the output of the second isolation amplifier (Q3021) provides a non-reflective source impedance to the mixer. Without the attenuator, mixer conversion loss could vary from unit to unit.

The harmonic mixer, consisting of diode CR2021, inductor L2014, and a half-wavelength (at 2182 MHz) transmission line, produces the difference frequency between the third harmonic of the 719 MHz oscillator frequency and the 2182 MHz reference frequency (nominally 2157 MHz). Note that the 2182 MHz signal is supplied from the 2182 MHz 2nd Local Oscillator through coaxial connector P237 and the power divider consisting of resistors R1021, R1023, and R1022 to the half-wavelength transmission line. The VCO input to the mixer switches diode CR2021 at a 719 MHz rate. The 2182 MHz reference acts as the RF and is applied to the diode from the transmission line. The resultant 25 MHz intermediate frequency is diplexed from the mixer through the 100 MHz low-pass filter consisting of capacitor C3014 and inductor L3014. (Diode CR2021 is mounted in printed circuit board cut-outs to relieve any necessity of bending the diode leads. Lead bending may fracture the diode case.) Inductor L2014 provides a bias return path to allow the diode to switch at a 719 MHz rate.

From the harmonic mixer, the signal is applied through the above mentioned lowpass filter to cascaded amplifiers U1053 and U1044B. These amplifiers boost the −32 dBm mixer output signal to a level appropriate to drive the phase/frequency detector. Amplifier IC U1053 contains two differential amplifiers in cascade; amplifier IC U1044 con-

tains only one differential amplifier and acts as a buffer. When the loop is first acquiring lock, such as at power-on, the nominal 25 MHz IF may be as high as 34 MHz. Two stages of amplification are necessary to ensure enough gain for the phase/frequency detector to drive the IF back to 25 MHz; the buffer is necessary to provide ECL levels to the detector.

The second input to the phase/frequency detector is the 100 MHz frequency from the reference oscillator in the 3rd converter via coaxial connector P235. This signal is applied through two amplifier stages, U1022A and U1022B, to a divide-by-four circuit, U1036A and U1036B. These two flip-flops divide the 100 MHz frequency to 25 MHz for applica- tion to the phase/frequency detector. (Two stages of amplification are used to isolate the 100 MHz reference bus from signals, generated in the local oscillator section of the 2nd Converter.) This stable 25 MHz reference output is used to lock the difference frequency from the harmonic mixer at 25 MHz.

The phase/frequency detector effectively measures the phase difference between the 25 MHz reference and the IF from the harmonic mixer, and determines the correction voltage that is to be applied to the 719 MHz VCO. This cir- cuit consists of two D-type flip-flops, U2047A and U2047B, and a differential amplifier stage used as a NAND-gate (U1044A). The 25 MHz reference signal from the frequency divider is applied to the clock input of flip-flop U2047A; the nominal 25 MHz signal from the harmonic mixer is applied to the clock input of flip-flop U2047B. The rising edge of the input signal to each flip-flop causes the $\overline{Q}$ outputs to return to the low level only after both flip-flops have been clocked.

If the harmonic mixer output frequency is below 25 MHz, (or if its phase lags that of the 25 MHz reference) the $\overline{Q}$ output of flip-flop U2047A will be high longer than that of flip-flop U2047B. If the harmonic mixer output frequency is above 25 MHz (or if its phase leads), the opposite will be true. When the two flip-flops are clocked at the same fre- quency and phase, the two outputs will be high for the same amount of time. From the two flip-flops, the $\overline{Q}$ outputs are applied to compensation amplifier U3053, a differential am- plifier that determines which output is high for a longer time.

Compensation amplifier U3053 provides part of the loop gain to ensure that the gain will be high enough to cause the 719 MHz oscillator to track the sweep of the 2182 MHz ref- erence oscillator. In addition, the compensation amplifier limits the loop bandwidth to 100 kHz to make certain that the loop will not oscillate. Note that the differential inputs to the amplifier each include a lowpass RC filter (R3041 and C3042 for the minus input; R2048 and C2055 for the plus input) to attenuate the undesired high frequency clock pulses from the phase/frequency detector.

The nominal swing of the U3053 output is from +12 to −12 volts. Since the compensation amplifier is capable of considerably more output swing than is needed to control the oscillator, a voltage divider is used to limit the output and reduce amplifier related noise. This voltage divider, con- sisting of resistors R2053, R2054, R3051, and R3052, re- duces the possible ±12 volt swing to +5 V to +12 V, as required by varactor diode CR1011. Nominal voltage in a locked condition is +6.75 to +7.5 V.

Thus, dependent upon whether the harmonic mixer out- put frequency is above or below 25 MHz, the correction voltage applied to diode CR1011 is higher or lower than nominal to drive the oscillator frequency in the required direction.

Front Panel 2nd Local Oscillator Output Circuit

A portion of each 2nd LO output signal is sent to the front panel 2nd LO OUT connector. This output provides signal for external accessory equipment, such as a tracking generator. Each local oscillator (719 MHz and 2182 MHz) output is applied through power dividers to a power combin- er for application to the 2nd LO OUT connector.

The 719 MHz oscillator frequency is applied from a pow- er splitter (R3027, R3028, R3029) through a 1 GHz low- pass filter (C3025, C2024, C1023, C1021, and three printed inductors), to the power combiner (R2024, R2025, R2026), and the front panel 2nd LO OUTPUT. The 2182 MHz oscil- lator signal is applied through a power splitter (R1021, R1022, R1023), a 2.2 GHz band-pass filter (consisting of coupled 1/4 wavelength printed lines) to the power divider (R2024, R2025, R2026) and the front panel 2nd LO OUTPUT.

Both 2nd local oscillator signals, 2182 MHz and 719 MHz, are present at the front panel when the 829 MHz 2nd Converter is selected.

719 MHz Output Circuit

The 719 MHz 2nd Local Oscillator signal is applied through divider resistors R2021, R2023, and R2024 to iso- lation amplifier Q2021. Q2021 boosts the signal level from about 0 dBm to +12 dBm to drive the 829 MHz mixer. The output of the amplifier includes a 3 dB attenuator (consisting of resistors R2027, R2026, and R2029), to ensure a 50 Ω non-reflective source impedance. The signal level at test point J2026 is typically −6 dBm.

◇4◇
110-MHz IF AMPLIFIER AND 3rd CONVERTER

The 110 MHz IF Amplifier and 3rd Converter accept the 110 MHz output from the 2nd Converters, amplify and convert the signal to a 10 MHz IF signal which is applied to the resolution circuits in the IF section. The 110 MHz signal is amplified in a three-stage gain block and applied to a three-section bandpass filter. This filter uses helical resonators and has a nominal bandwidth of 1 MHz. From the bandpass filter, the signal is applied to a mixer and heterodyned with a 100 MHz local oscillator signal to produce a 10 MHz third IF signal. The resulting signal, nominally at a level of −35 dBm at the top of the screen, then drives the Variable Resolution circuits.

Initial gain for the analyzer is provided by the 110 MHz IF Amplifier. This gain compensates for signal level losses in the three mixers. Three stages of amplification are used, plus a pin diode controlled attenuator that allows for adjustment of the gain. Typical gain for the amplifier is 21 dB. From the amplifier, the 110 MHz signal is applied to the 3rd Converter through a bandpass filter.

The filter is a three section unit using helical resonators. Its bandwidth of 1 MHz defines the broadest resolution bandwidth of the analyzer, provides good image rejection, and limits noise in the frequency spectrum in which desirable signals appear.

Consisting of a mixer, an oscillator, and various output amplifiers, the 3rd Converter converts the 110 MHz second IF signal into the 10 MHz third IF signal. The local oscillator is a crystal controlled circuit that generates a precise 100 MHz signal. This 100 MHz is applied to the mixer and to output amplifiers. The 100 MHz signal is used in the 2nd Converter and the phaselock section. It is also furnished to a front panel CAL OUT connector for external use.

The mixer is a diode ring type that is fed from balanced drivers which are driven by the 100 MHz oscillator. From the mixer, the output signal, at 10 MHz, is applied to the Variable Resolution section of the 3rd Converter.

110 MHz IF AMPLIFIER ◇16◇

The 110 MHz IF Amplifier consists of three stages of amplification and an attenuator. Since the first two mixers in the RF system offer no high frequency gain, it is important that this amplifier exhibit low noise characteristics. Also, it must be relatively free from third-order intermodulation distortion.

Signal input to the amplifier is from the 2nd Converter through coaxial connector P321. This signal is nominally 110 MHz and is applied to an impedance matching bandpass filter consisting of inductor L2044 and capacitor C325. The signal is injected into the parallel tuned circuit through a tap in the inductor and taken out at the high impedance side through another variable capacitor, C2047. Inductive input provides for converting to high impedance within the tuned circuit; the extra capacitor on the output provides for converting back to 50 Ω nominal. The primary tuning capacitor (C325) adjusts the resonant point; the output capacitor (C2047) is adjusted in combination with C325 for good impedance match at 110 MHz. This is done using a return loss bridge. The nominal return loss is 35 dB. The Q of the input filter is approximately 20.

From the input filter, the signal is applied to Q4053, the first stage of amplification. This is a broadband feedback amplifier to provide good input and output impedance and controlled gain. All feedback is through reactive components (transformer T3054) not resistive components. Thus, the impedance and gain can be controlled without significant noise problems.

The second amplifier stage, Q4037, is essentially the same as the first, with only minor bias differences. Gain through each of these stages is approximately 9 dB. The output is applied through a 3 dB attenuator, to preserve the impedance figure, to the bridged T adjustable attenuator. The 3 dB attenuator consists of resistors R2039, R2038, and R2043.

From the 3 dB attenuator, the signal is capacitively coupled through C2037 to the adjustable attenuator. This attenuator uses two PIN diodes (CR3030 and CR1029) in the mode in which the resistance to RF signal flow is controlled by the current through the diodes. Refer to Fig. 5-8 as an aid in understanding the following description.

With reference to Fig. 5-8, if resistor R1 were set to infinite resistance and resistor R2 were set to zero resistance, the RF signal path would be through R2 to ground, thereby producing infinite signal attenuation. If resistor R1 were set
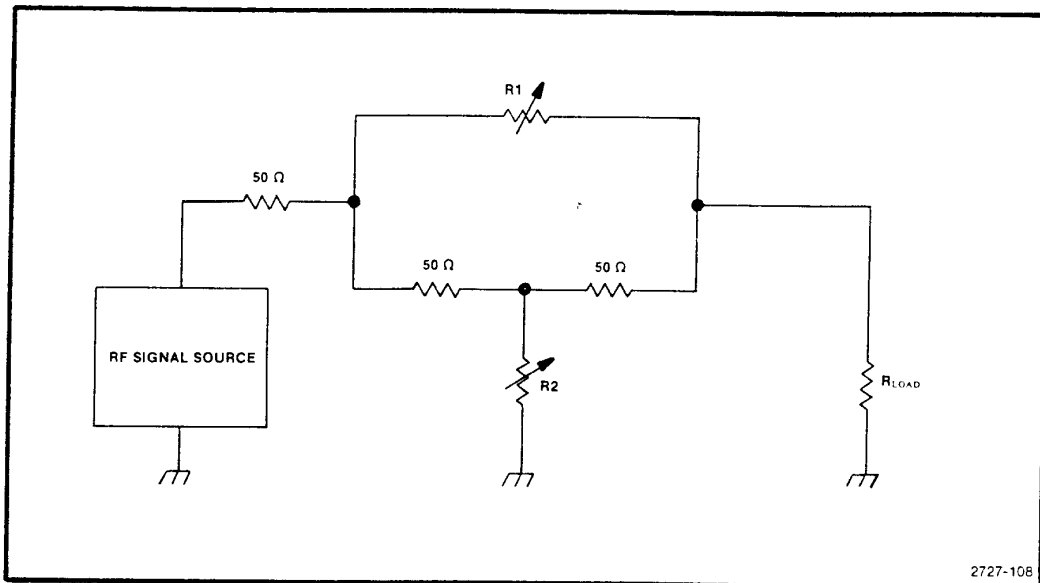
Fig. 5-8. Bridged T attenuator equivalent schematic.

to zero resistance and resistor R2 were set to infinite resistance, the RF signal path would be through R1 to the load, thereby producing almost no attenuation. This, basically, is how the adjustable attenuator operates, except that resistors R1 and R2 are actually PIN diodes and the RF path resistance through these diodes is controlled by the current through the diodes in an inverse proportion (higher current results in less resistance to RF).

With reference to Diagram 16, resistors R3035 and R2030 establish a constant current of approximately 2 mA from the −15 volt supply to the diodes. This current is divided according to the bias on the diodes. The bias, in turn, is established by gain adjustment R1015, from the +15 volt supply. If R1015 is set low (near ground), diode CR3030 is reverse biased and the 2 mA flows through diode CR1029. This routes the RF signal through resistors R2032 and R3029 and capacitor C2029, with the impedance characteristics of CR1029 added for maximum attenuation.

If R1015 is set higher (nearer +15 V), diode CR3030 is forward biased and starts to conduct. Since the 2 mA supply current is relatively constant, this subtracts from the current through CR1029. Thus, the impedance of the diodes is relatively constant, resulting in a good impedance match over a broad range. Dependent upon the exact amount of current through CR3030, part of the RF signal path is through that diode to the output amplifier and part is through R2032 and diode CR1029 to ground. This results in reduced signal attenuation.

If R1015 is set to the positive limit, the entire 2 mA flows through CR3030. This routes the RF signal through CR3030 (which exhibits little resistance with high current) to the output amplifier with almost no attenuation. (The insertion loss is approximately 1 dB.)

From the adjustable attenuator, the signal is applied to the final amplifier Q3018. This stage is a broadband feedback amplifier that supplies relatively substantial output current and exhibits good intermodulation distortion performance. This is provided primarily through the large current capacity, by negative feedback through resistor R3014, and emitter degeneration through resistor R4029. These resistors are sized to provide a resonably good impedance match at 110 MHz. Nominal gain of the stage is 13 dB.

With Gain potentiometer R1015 set for maximum gain (least attenuation) the gain of the 110 MHz IF Amplifier is approximately 26 to 27 dB. The Gain potentiometer is normally adjusted for total gain of 21 dB.

The output signal from the 110 MHz IF Amplifier is applied to the 110 MHz Bandpass Filter.

110 MHz BANDPASS FILTER

⟨11⟩ ⟨16⟩ ⟨18⟩

The 110 MHz Bandpass Filter is a three-section filter using helical resonators, the major function of which is to de-

determine the widest resolution of the analyzer. Another filter function is to provide image rejection (that is, to prevent the mixer from producing 10 MHz outputs from input signal of 90 MHz). Still another function is to limit the noise spectrum appearing at the 10 MHz IF circuits to those frequencies at which signals also appear.

Though the filter is a sealed unit, in the interest of system understanding, the following brief description is provided.

The filter consists of three small helical resonators enclosed in cans and tuned with multi-turn trimmer capacitors. For purposes of impedance matching, the filter is symmetrical. The end resonators are connected to external circuits by 10 picofarad capacitors attached to taps on the coils. Coupling between resonators is accomplished through holes in the resonator cans.

Adjustment of the filter for minimum attenuation is performed at calibration by setting the three trimmer capacitors. Insertion loss is on the order of 4 to 4.5 dB.

From the filter, the 110 MHz signal is applied to the 3rd Converter.

◇④◇

3RD CONVERTER

Refer to Diagram 4 and to the block diagram adjacent to Diagram 17. The 3rd converter converts the 110 MHz IF signal to 10 MHz for application to the Variable Resolution circuits. It also generates the 100 MHz signal for the 3rd Converter, the front panel CAL OUT signal, and the 110 MHz reference for most of the phaselock loops in the analyzer. The circuits consist of an oscillator and driver, four identical reference output amplifiers, a mixer, and a calibrator output amplifier.

Refer to Diagram 17 while reading this description.

Oscillator/Driver Circuit

The oscillator Q3041 is of the Colpitts configuration with a 100 MHz microwave type crystal operating in the series resonant mode in the feedback loop. That the crystal is a microwave type indicates that it is not only a high-Q type, but that it is mounted at three points to alleviate mechanical vibration problems. (The components inside the dashed line immediately below crystal Y3036 in Diagram 17 are included for future use only and are not described here.) Tuning capacitor C3031 in the collector circuit serves to adjust for maximum output.

From the oscillator collector circuit, the output is RC coupled to driver stage Q2036. The driver is a feedback amplifier that provides output power on the order of +10 dBm to drive all of the reference amplifiers plus the mixer amplifier. The output is transformer coupled from the collector circuit.

Reference Amplifier Circuits

The reference output circuits consist of four identical low-gain common emitter amplifiers with relatively high levels of emitter degeneration. These are transistors Q4018, Q2015, Q3015, Q2016 and associated components. The primary purpose of these amplifiers is to provide isolation among the reference outputs and isolation of those outputs from the oscillator and mixer circuits. The output of each is approximately 0 dBm.

From amplifier Q4018, the output is applied to the 829 MHz IF circuits through coaxial connector J2013. From amplifier Q2015, the output is applied to coaxial connector J2012 and is reserved for future use. From amplifier Q3015, the output is applied to the Phaselock Synthesizer circuits through coaxial connector J1023. From amplifier Q2016, the output is applied to coaxial connector J4027 and is reserved for future use. The Q2016 output is also coupled to the Calibrator Output Amplifier.

Mixer Circuit

The mixer circuit combines the 100 MHz oscillator frequency with the 110 MHz IF signal from the 110 MHz Bandpass Filter to produce the 10 MHz IF output signal. From transformer T2026 of the driver circuit (Q2036), the 100 MHz signal is applied to transformer T2041, which converts the single-ended driver output to a balanced signal to drive the push-pull amplifier that drives the mixer. This amplifier consists of transistors Q1048 and Q2046 and provides a balanced signal, coupled through transformer T3053 to diode ring mixer CR2054. The signal level of the 100 MHz, applied to the mixer, is approximately 100 milliwatts to provide adequate intermodulation distortion performance. The 110 MHz IF, through Bandpass Filter (FL36), is applied through coaxial connector J2058, the impedance matching LC circuit that consists of inductor L1055 and capacitor C1056, and transformer T1053, to the mixer.

The 10 MHz output from the center tap of T1053 is applied through a diplexer and coaxial connector J3057 to the Variable Resolution circuits. Loss through the mixer is typically 9 dB. The input level from the 110 MHz bandpass filter is nominally −26 dBm and the output to the Variable Resolution circuits is nominally −35 dBm.

Calibration Output Amplifier

The calibrator output amplifier is a differential amplifier (Q2031 and Q1031) that is overdriven. With low levels of drive, this amplifier would operate as a small-signal amplifier. However, with the higher positive and negative levels from reference amplifier Q2016, the transistors are either driven hard or are not conducting at all. Since the transistors are overdriven, the current in the output side (Q1031) is the dc bias current when that side is conducting. Changing the bias current will therefore change the output voltage. Thus, the output is determined by internal dc levels, not input signal levels. Potentiometer R1045 provides for adjustment of that quiescent current.

The output frequency is stable and rich in harmonics. Thus, it provides a useful signal comb of 100 MHz markers to approximately 2 GHz. At 100 MHz, the output level is set by R1045 for −20 dBm which is applied to the front panel CAL OUT connector through coaxial connector J1015.

⟨5⟩
IF SECTION

The IF section receives the 10 MHz IF signal from the 3rd Converter, establishes the system resolution through selective filtering, levels the gain for all bands, and logarithmically amplifies and detects the signal to produce the video output to the Display section.

System resolution is selectable, under microcomputer control, among five bandwidths: 1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz. (Some 30 Hz circuits are included for future use.) This selection is done in the Variable Resolution circuit block by two sets of filters. Bandpass filters are also included at the circuits input and output.

Significant gain is provided in the resolution circuit block by several stages of amplification. Also, the capability to add other gain steps under microcomputer control is provided by switching attenuators in or out of the signal path. These attenuators, by being switched in combination, provide for 10, 20, 30, or 40 dB of additional gain.

Leveling to compensate for instrument front-end losses is also included in the resolution circuit block. Front-end losses occur primarily in the higher frequency bands; therefore, most band leveling amplification is required in those bands.

In order that each division of signal change on the crt screen be equal to that for each other division and be equvalent to a similar signal level change in dB, a logarithmic amplification of the signal is required. This is done by a seven stage amplifier that produces an output that is proportional to the logarithm of the input. Thus, the screen displacement can be selectable as to amount of change per divisions, and can be proportional to the input level change. For instance, in the 10 dB per division mode, each division of displacement in the screen represents a signal level change of 10 dB regardless of whether it is at the top or bottom of the screen.

Following the logarithmic amplifier, an area detector produces a positive-going pulse output that is applied to the display section as the VIDEO signal.

Variable Resolution Section
⟨18⟩ ⟨19⟩ ⟨20⟩

The Variable Resolution (VR) circuits provide selection of resolution bandwidth under microcomputer control, and approximately 35 dB of system gain. It consists of two sets of filters and various gain leveling stages. Since the input to the VR circuits is nominally at −35 dBm and the Log Amplifier input must be 0 dBm for full screen, the VR circuits must provide the gain difference. Also, additional gain (up to 40 dB) is required for operation in the 2 dB/DIV or the linear mode plus compensation for variations in front end losses.

Physically, the VR section consists of two sub-assemblies that plug onto the analyzer mother board. The input circuits are in one sub-assembly; the output section and digital interface are in the other. Each of the sub-assemblies consists of boards that plug onto a four-layer mother board with a ground plane on both outside layers. Only power supply and control voltages travel through the mother board. All signal interconnection is via coaxial cable.

Circuits for the VR section are contained on three diagrams: 18, 19, and 20. The following paragraphs describe the circuits.

Input Circuit ⟨18⟩

The VR Input circuit receives the −35 dBm 10 MHz signal from the 3rd Mixer through J693. This signal is applied to a two-pole, 1.2 MHz bandpass filter that augments the 1 MHz filter that precedes the 3rd Mixer and provides initial selectivity. This 1.2 MHz filter includes C1037 and C1031 and all of the components between. Filter tuning is provided by variable capacitors C1033 and C1026.

From the filter, the signal is applied to broadband feedback amplifier Q1023, which is biased at a relatively substantial output current (approximately 50 mA) to exhibit good intermodulation distortion performance. This performance is provided primarily through the large current capacity, by negative feedback through resistor R1025 and by emitter degeneration resistor R1023.

At the output of amplifier Q1023 is a 6 dB attenuator that provides a clean 50 Ω output to the 1st Filter Select circuits and reflects a 50 Ω termination back through the amplifier for proper termination of the 1.2 MHz bandpass filter. The output signal is transmitted via jumper B.

1st Filter Select Circuit ⟨18⟩

The VR 1st Filter Select circuit operates in conjunction with the 2nd Filter Select circuit to determine the overall system bandwidth through banks of switched filters that are selectable under control of the analyzer microcomputer. Data bits 0, 1, and 2 from the data bus are applied to decimal decoder IC U4035, which enables the selected filter by providing a low signal on the appropriate output pin. Bandwidth selections are 1 MHz to 100 Hz in decade steps. (Note that 100 Hz resolution is part of Option 03.) The data bits select a filter bandwidth according to Table 5-4.

Table 5-4
BANDWIDTH SELECTION

DB0	DB1	DB2	Bandwidth
1	0	0	1 MHz
0	1	0	100 kHz
1	1	0	10 kHz
1	0	0	1 kHz
1	0	1	100 Hz
0	1	1	30 Hz (for future use)

Selection of filters is done by PIN diode switching. At the input and output of each filter is a series and a shunt diode. When a filter is selected, the series diodes are biased on and the shunt diodes are biased off. For the filters that are not selected (only one is on at a time), the diode conditions are opposite. Since the switching operation is the same for all filters, the following description of the 100 kHz filter selection is applicable to all with appropriate component designators.

If we assume a content of 010 for the three data bits, line 2 from U4035 will be low. This will turn on transistors Q3019

and Q3055, which operate as dc switches. With input switch Q3019 turned on, the current path is through R4012, L3012, CR3010, L3013, R3014, and Q3019. This current is determined by decoupling resistor R3014 and resistor R4012, which is common to all filters, and is sufficient to turn CR3010 on enough that it appears to be merely a resistor to RF. At the same time, the voltage drop across R4012 is sufficient to reverse-bias CR3012. The same operational situation exists for the filter output switch, Q3055. Resistors R3057 and R1067 establish the current to forward-bias CR3061 and reverse-bias CR3060.

Thus, the signal from the Input circuit via jumper B is applied through the selected filter and transmitted to the 10 dB Gain Steps circuit via jumper K. Nominal loss through the filter circuit is approximately 13 dB, with slight variations among the filters. The output level is nominally −32 dBm at 100 kHz.

In the non-selected filter sections, the input and output switch transistors are turned off by the high outputs from decimal decoder U4035. The collectors are pulled toward −15 V by pulldown resistors, thus forward biasing the shunt diodes (input: CR3014, CR2013, CR2011, CR1013, and CR1011; output: CR3062, CR2066, CR2055, CR1055, and CR4065). Since one filter is always selected, the voltage drop across the common input and output resistors (R4012 and R1067, respectively) provides for back biasing the series diodes (input: CR3011, CR3012, CR2010, CR1012, and CR1010; output: CR4068, CR2062, CR2059, CR1059, and CR4064). Note that input and output switching is provided on the board for future use with 30 Hz resolution.

Design of the filter for each bandwidth is determined by the requirements of each band and ranges in complexity from no filter at all to a complex two-crystal arrangement.

In the 1 MHz section no filter is used, because this circuit section is preceded by two filters that accomplish the required function. The first is the 1 MHz filter between the 2nd and 3rd Converters; the second is the 1.2 MHz filter in the VR Input circuit. Instead of a filter, a 6 dB attenuator is contained in the 1 MHz selection circuit. This attenuator provides initial leveling to compensate for less loss because no filter is used.

The 100 kHz filter is a double-tuned LC circuit that is designed for a good time-domain response shape. Variable capacitors C3023 and C3035 provide for input and output adjustments. Impedance matching is accomplished at both input and output by series capacitors C3020 (input) and C3048 (output).

The 10 kHz filter uses a pair of two-pole monolithic crystal filters that are interconnected by variable shunt capaci-

tor C2037. Input and output impedances are matched with broadband transformers T3026 and T3055. A 3 dB attenuator, consisting of R2027, R2026, and R2028, is included at the filter input.

The 1 kHz resolution filter consists of a single two-pole monolithic crystal filter, matched to the 50 Ω impedance with broadband transformers T2035 and T2055. A 2 dB attenuator, consisting of R2024, R2023, and R2025 is also part of the filter.

The 100 Hz filter uses a pair of high Q crystals in a balanced two-pole ladder configuration. These crystals are matched for both frequency and temperature characteristics. Input and output impedance matching is accomplished primarily by transformers T1025 and T1039. Two small capacitors in the same transformer circuit as the crystals (C1030 and C1035) are adjustable to cancel the parallel capacitance effect of the crystals. Also, a 2 dB attenuator is included at the filter input and consists of resistors R1026, R1028, and R1027.

10 dB Gain Step Circuit ⟨18⟩

The 10 dB Gain circuit provides 10 dB of signal gain when selected by the microcomputer. The circuit consists of three stages of amplification, one stage provides variable gain, the other two are fixed gain steps. The nominal input signal level from the 1st Filter Select circuit is −32 dBm for a resolution bandwidth of 100 kHz. (All levels listed in this description relate to the 100 kHz resolution.)

The input signal is applied through an impedance transformer, T3019, to the first amplifier stage consisting of a differential pair (Q3016 and Q2027) and an emitter follower output amplifier (Q1036). Negative feedback through R1031 and R2051, provide gain stabilization. An output resistor, R2035, increases the output impedance of the composite amplifier to approximately 50 Ω.

Gain of the input stage is fixed for all resolution bandwidths except 30 Hz. (In instruments that may have the 30 Hz resolution bandwidth capability, the gain for 30 Hz will be set to a precise level by activating Q2015. Transistor Q2015 is biased on by a low on pin L. This adds R2025 (30 Hz level) across feedback resistor R2051. Adjustment R2025 can now set the gain of the stage.)

The output from the 1st stage is then applied to a common emitter stage (Q2043). Gain of this stage, when transistor Q4039 is turned on, is 10 dB. When the base of Q4039 is pulled low by data bit 0 from Q4035 on the VR mother board #1, the transistor saturates and shunts the emitter load resistor R3048 with R3038 and the 10 dB Gain adjustment R3035.

The output of Q2043 drives the input of the third amplifier stage. This stage operates the same as the first stage except for gain variation. Feedback resistor R1060 is shunted by PIN diode CR1053. As the current through the diode increases, the resistance decreases and the gain of the stage increases. Gain control of the stage is established by the setting of the front panel AMPL CAL adjustment. Gain range is about 14 dB.

Output impedance of the stage is 50 Ω, set by resistor R1064. Nominal output level is −10 dBm for a full screen display. This level may be as high as +0 dBm when MIN NOISE is active. 10 dB of gain is also removed from the Log Amplifier to reduce the noise level and must be supplied by the VR section.

20 dB Gain Steps Circuit ⟨19⟩

The 20 dB Gain Steps circuit provides −6 dB, +4 dB, +14 dB, and +24 dB of gain in precise 10 dB steps. The nominal −10 dBm input is supplied through pin P from the 10 dB Gain Steps circuit. This signal is applied to a chain of three common-emitter amplifiers, each using emitter degeneration. Changing the emitter resistance is used to change amplifier gain under the direction of the microcomputer.

The nominal gain of the complete circuit is −6 dB, with Q2018, Q2042 and Q1062 biased off. This provides a nominal −16 dBm output. In this condition, control pins V and Y are high, causing switching transistors Q2018, Q2042, and Q1062 to be cut off.

When pin V is low, Q2018 and Q2042 are saturated, raising the total gain of the first two amplifiers 20 dB. Variable resistor R2023 is used to adjust the gain shift of the first stage (Q1025) while the gain shift of the second stage (Q1035) is fixed at +10 dB. This adjustment allows the gain shift to be exactly set to +20 dB.

When pin Y is low, Q1062 is saturated, raising the gain of the third amplifier (Q1043) by 10 dB. Variable resistor R1063 allows the gain shift to be exactly set to +10 dB.

Data bits 2, 1, and 0 control the gains of the 10 dB Gain Steps circuit and the 20 dB Gain Steps circuit. Bit 2 controls pin V, bit 1 controls pin Y, and bit 0 controls pin N. The data is decoded and stored in latches on the VR mother board #2. Table 5-5 shows the state of bits 2, 1, and 0 and the gain shifts of amplifier stages Q2043, Q1025, Q1035, and Q1043.

The output of the 20 dB Gain Steps circuit is attached to coaxial connector J684. The signal is routed through a double coaxial cable to the Band Leveling circuit.

Table 5-5
GAIN STEP COMBINATIONS

Required Gain Addition	Data Bits			10 dB Gain Steps Circuit		20 dB Gain Steps Circuit			
	2	1	0	Q2043	Pin N	Q1025+Q1035	Pin V	Q1043	Pin Y
10 dB	0	0	1	10 dB	0	0 dB	1	0 db	1
20 dB	1	0	0	0 dB	1	20 dB	0	0 dB	1
30 dB	1	0	1	10 dB	0	20 dB	0	0 dB	1
40 dB	1	1	1	10 dB	0	20 dB	0	10 db	0

Band Leveling Circuit ⟨19⟩

The two amplifiers in the VR Band Leveling circuit correct the gain variations caused by the front end. These band-to-band variations are caused by mixing of different harmonics in the 1st converter and losses from the preselector.

The output level of this board is −8 dBm while the nominal input is −16 dBm. This input level occurs on band 1 (at 100 kHz resolution in Min Distortion mode) but decreases in the higher bands; the output is kept constant by using the microcomputer to adjust the amplification for each band.

The two amplifier blocks in this circuit are similar to the blocks in the 10 dB Gain Steps circuit. The block is a three-transistor circuit using a differential pair connected to an emitter-follower. The gain is controlled by altering the feedback network.

From the 20 dB Gain Steps circuit, the signal is applied through a double-shielded coaxial cable and J683. It is sent through input transformer T2013 to the first amplifier block.

The first block (Q2015, Q2019, and Q1025) has a gain range of 13.5 dB by using a PIN diode (CR2021) in the feedback loop. The bias for this diode comes from an array of variable resistors on the VR mother board #2, with the individual resistor selected by the microcomputer.

The second block is similar except that the gain change occurs in one step of approximately 12.5 dB. This gain step occurs only in the higher bands and is activated by the microcomputer through user-selected diodes on the VR mother board #2.

The 492/492P is normally calibrated with the band 1 gain control resistor set for minimum gain. Gain is then added as required for the higher bands. Data bits 6, 5, 4, and 3 control band selection.

The output from the second amplifier block is applied through connector EE to the VR 2nd Filter Select circuit.

2nd Filter Select Circuits ⟨20⟩

The VR 2nd Filter Select circuit operates in conjunction with the 1st Filter Select circuit to determine the overall system bandwidth through banks of switched filters that are selectable under control of the analyzer microcomputer. Data bits 0, 1, and 2 from the data bus are applied to decimal decoder U3070, which enables the selected filter by providing a low signal on the appropriate output pin. Bandwidth selections are 1 MHz to 100 Hz in decade steps.

Note that 100 Hz resolution is part of Option 03. Also note that, although the 2nd Filter Select circuit is similar to the 1st Filter Select circuit, no 30 Hz switching circuits are included on the board for future use. When 30 Hz resolution is incorporated, the 30 Hz bandwidth will use the 1 kHz filter in the 2nd Filter Select circuit. This can be seen in the connection between pins 5 and 7 on decimal decoder U3070, thus resulting in line 5 being low for both 1 kHz and 30 Hz bandwidth sections.

The data bits select a filter bandwidth as described in Table 5-4. Filter selection is accomplished as described for the 1st Filter Select circuit.

Thus, the signal from the Band Leveling circuit via jumper EE is applied through the selected filter and transmitted to the Post VR Amplifier circuit via jumper JJ. Nominal loss through the filter circuit is approximately 13 dB, with internal adjustment compensation for slight variations among the filters. The output level is nominally −21 dBm.

Table 5-6
PROGRESSION OF GAIN REDUCTION

Input Level	Point 1	Point 2	Point 3	Point 4	
		Beyond Logging Range			
X−10 dB	0.00316	0.01	0.316	0.1 ⌐	
					−0.216
X Level	0.01	0.316	0.1	0.316 ⌐	
					−0.684
X+10 dB	0.0316	0.1	0.316	1.0 ⌐	−0.684
			⌐—0.684—⌐		
X+20 dB	0.1	0.316	1.0	1.684 ⌐	−0.684
		⌐—0.684—⌐	⌐—0.684—⌐		
X+30 dB	0.316	1.0	1.684	2.368 ⌐	−0.684
	⌐—0.684—⌐	⌐—0.684—⌐	⌐—0.684—⌐		
X+40 dB	1.0	1.684	2.368	3.052 ⌐	−0.684
X+50 dB	3.16	Beyond Logging Range			

Switching in the other, non-selected filter sections, is accomplished as described in the 1st Filter Select circuit paragraphs. Also as described in those paragraphs, the design of the filter for each bandwidth is determined by the requirements for each band and ranges from no filter at all to a complex two crystal arrangement. An important design difference is that the 2nd Filter Select circuit contains a variable resistor in the attenuator that follows the input switch in all except the 100 kHz circuit. The purpose of this adjustment is to allow calibration of all other circuits to match the 100 kHz circuit. The Band Leveling circuit furnishes compensation gain to obtain equal signal levels for all bands. Thus, the calibration is required only to remove variations between the filters by adjustments R1065, R3035, R3025, and R3015.

It is in the 1 MHz section that no filter is used. This is because this circuit section is preceded by the 1 MHz (wide) filter between the 2nd and 3rd Converters and the 1.2 MHz filter in the VR Input circuit. Those filters accomplish the required function. Thus, instead of a filter, an attenuator that includes the calibration adjustment is contained in the 1 MHz selection circuit. This attenuator compensates (offsets) the gain loss associated with a filter in the other resolution circuits.

The 100 kHz filter is a double-tuned LC circuit that is designed for a good time-domain response shape. Variable capacitors C2050 and C5055 provide for filter tuning. A 6 dB attenuator (resistors R2048, R2047, and R2049) is included at the filter input. This attenuator and the filter form a reference to which the levels of the other circuits are calibrated. Impedance matching is accomplished at both input and output by series capacitors C1047 and C6052.

The 10 kHz filter uses a two-pole monolithic crystal filter. The impedances at the input and output are matched to 50 Ω by T4040 and T6045. An attenuator that contains the calibration adjustment is included at the filter input for filter variation compensation.

The 1 kHz filter also uses a two-pole monolithic crystal filter with impedance matching transformers T5030 and T6040 at the input and output. An attenuator that contains the calibration adjustment is included at the filter input for filter variation compensation.

The 100 Hz filter uses a pair of high-Q crystals in a balanced two-pole ladder configuration. These crystals are matched for both frequency and temperature characteristics. Input and output impedance matching is accomplished primarily by transformers T4019 and T7015. Two small capacitors in the same transformer circuit as the crystals (C6011 and C7011) are adjustable to cancel the parallel capacitance effect of the crystals. An attenuator that contains the calibration adjustment is included at the filter input for filter variation compensation.

Post VR Amplifier Circuit ◇20◇

The Post VR Amplifier circuit provides the final VR system gain to bring the signal to the required output level and provides the final bandpass filtering to assure clean performance. The circuit consists of two stages of gain followed by a filter.

From the 2nd Filter Select circuit, the signal is applied through jumper JJ to the input of common emitter amplifier

transistor Q2056. The circuit includes potentiometer R2038 in the emitter circuit to allow for adjusting the post VR amplifier gain. The output is transformer coupled by T1059 to the base of feedback amplifier transistor Q1048. This circuit includes emitter degeneration through resistor R2042 and collector-to-base feedback through resistor R1052. The collector feedback is used in this instance to help provide a well-defined output impedance of 50 Ω. Input impedance to this stage is defined by transformer T1059 and resistor R1058 across the primary.

This final VR amplifier stage is biased for relatively high output current. This is required because the VR system is sometimes driven at an increased output level of +10 dBm, and more current is required to prevent gain compression. A higher output level is required in low noise or low intermodulation distortion operation to compensate for the 10 dB of gain that is switched out of the Log Amplifier.

From the final amplifier, the signal is applied through the 1.2 MHz bandpass filter that consists of capacitors C2033 and C2018 and the components between. This filter is a double-tuned design and has an insertion loss of approximately 2 dB.

As an aid to understanding the overall VR system functions, it is helpful to understand some aspects of filter design. When designing a wide-bandpass filter, on the order of ten percent or greater, stop-band attenuation becomes a severe problem in two-pole filters. The result is that a given filter design will degenerate into either a high-pass or a low-pass filter. The design of the filter in the Post VR Amplifier circuit degenerates into a low-pass unit. However, since the VR system includes a bandpass filter at both the input and the output, and since the input filter in the VR Input circuit degenerates into a high-pass unit, the overall VR system exhibits clean stop-band performance.

The output signal from the filter is applied through coaxial connector J682 to the Log Amplifier. The output level is nominally at 0 dBm.

Digital Control Circuits ⟨19⟩

The Digital Control circuits provide address and data decoding for the bandwidth and gain step selection and band identification for the band leveling gain control, and provide the control signals to the other sections of the VR system to accomplish those tasks.

Address and data valid lines from the analyzer address bus are applied to address decoder U4022 through connector P1049 pins 9, 10, 12, 13, 14, and 20. Data bit 7 is also applied through P1049 pin 7 as a supplemental address bit to select between the latch that stores data for bandwidth selection, and the latch that stores data for band identification and gain step selection.

Data lines from the analyzer data bus are applied through connector P1049 pins 1, 2, 3, 4, 5, 6, and 8 to data latches U3010 and U3017. Note that only data bits 0, 1, and 2 are applied to latch U3010.

Latch U3010 stores the data that selects among the filters in the 1st and 2nd Filter Select circuits. Outputs from pins 2, 19, and 16 of U3010 are applied to the decimal decoders in the filter select circuits through edge connector pins G, F, and E to control the filter selection. Decoding is done within the filter select circuits because it results in fewer lines between circuits and provides extra buffering to reduce noise transmission between circuits.

Latch U3017 stores the data that select among the various gain steps and that identify the selected frequency band for control of the band leveling function. Outputs from pins 2, 5, and 6 (corresponding to data bits 0, 1, and 2) are applied to inverter transistors Q4035, Q3035, and Q4037, respectively. From Q4035, the output signal is applied through connector P1049 pin 32 to the 10 dB Gain Steps circuit to control gain switching. From Q3035, the output signal is applied through edge connector pin 25 to the 20 dB Gain Steps circuit to control switching of the 10 dB gain switch; from Q4037, the output signal is applied through edge connector pin 27 to the 20 dB Gain Steps circuit to control switching of the 20 dB gain step.

Outputs from latch U3017 pins 15, 16, 19, and 12 (corresponding to data bits 3, 4, 5, and 6) are applied to band decoder U3023, an open collector decoder. If band 1 is selected, pin 1 output is low. These outputs are used in conjunction with a 7.5 volt reference source, provided by operational amplifier U3038B and driver transistor Q3036, to produce signals that are applied to a second operational amplifier (U3038A). These signals correspond to the amount of gain that must be supplied for each band to level the output for all bands. The analog output from U3038A is applied through edge connector pin BB to the gain control PIN diode in the Band Leveling circuit. For example; if band 1 were selected (U3023 pin 1 low), the current path is through potentiometer R2031 and the emitter of Q3036. From the potentiometer arm, the voltage is applied through resistor R2033 to the summing junction at the input to operational amplifier U3038A, driving that junction more negative. This shifts the output from U3038A more positive to increase the current through band leveling PIN diode CR2021. Potentiometer R2031 provides for calibrating the current through the PIN diode for band 1. In similar fashion, the other potentiometers (R3034, R3030, R3019, R3022, R3024, R3026, R3032, R3029, and R3028) allow for adjusting the current for each of the other bands.

Also, for bands 4 through 10, a diode may be connected to each decoder output to transmit that low signal via edge connector pin DD to the gain control transistor in the Band Leveling circuit to increase the gain in each of those bands. Those diodes are CR3022, CR3023, CR3024, CR3025, CR3031, CR3027, and CR3026, and are installed during final instrument calibration.

5 Volt Regulator Circuit ⟨19⟩

The 5 Volt Regulator circuit (U3041) supplies the required 5 volt source for use in several sections of the VR system. This is required because of noise in the 5 volt supply.

LOGARITHMIC AMPLIFIER AND DETECTOR ⟨21⟩

Refer to the block diagram adjacent to Diagram 21. The Logarithmic (Log) Amplifier and Detector accepts input signals from the VR circuits, with a dynamic range to 90 dB. It then amplifies these signals so the output is proportional to the logarithm of the input, and applies the signals to a linear detector to produce the video output signal. By controlling the compression curve characteristics, each dB of change in the input signal level results in an equal increment of change in the output. Thus, in the 10 dB/division mode, each division of displacement on the screen represents 10 dB of input signal level change.

Log Amplifier Circuits

The Log Amplifier circuits logarithmically amplify the input signal from the VR circuits and apply the output signal to the Detector circuit. These circuits consist of seven ac coupled amplifier stages. Each stage has two gain values that depend on signal amplitude. In addition, the first three stages have an extra automatically selected gain value. The combined circuits provide high gain for low-level signals and low gain for high-level signals. For the output signal to be proportional to the logarithm of the input, more gain is required for a change from −90 dBm to −89 dBm than a change from −1 dBm to 0 dBm. Thus, for a given stage of the seven, the gain starts at approximately 10 dB for a low-level signal and decreases to unity as the input signal level increases. In the first three stages, the gain becomes less than unity as the signal amplitude further increases.

Input signal levels nominally range between −90 dBm and 0 dBm. As the signal level increases, the gain decrease begins with the final stage and proceeds in succession back through the remaining six stages to the first. Since each stage produced approximately 10 dB of gain initially, and

that gain was reduced to unity, the total gain reduction is 70 dB. With further increases in input signal level, three more gain change steps take place. The gain of the first three stages is reduced below unity approximately 7 dB for each stage. This reduction starts with the first stage and proceeds to the third, to provide an additional gain reduction of approximately 20 dB.

Thus, as the input signal increases from −90 dBm to +10 dBm, the gain through the amplifier decreases logarithmically so that the output signal is exactly proportional to the logarithm of the input. This is accomplished through a system of series diode limiting in each stage, with a second set of diodes for extra limiting in each of the first three stages. Refer to Diagram 21 while reading the following.

The following description of a simple three-stage log amplifier with one gain step in each stage is provided as an aid to understanding the concept of a logarithmic amplifier. For the example amplifier shown in the following three figures and described in the text, the gain of each stage is 3.16 V (10 dB) up to an output level of 1 volt peak, then unity for output levels greater than 1 volt peak; that is, each stage uses one breakpoint. The breakpoint voltage is used for ease of illustration; the actual breakpoint voltage is significantly lower.

Figure 5-9 illustrates the amplifier and the input signal source. For purposes of discussion, assume that the source has a step attenuator at the output that will allow incrementing the input signal in 10 dB steps. Table 5-6 shows the progression of gain reduction above 1 volt at each amplifier stage output. Note that with each input level change of 10 dB, the output change at point 4 is 0.684 volt. The gain curve for one stage is illustrated in Fig. 5-10. Also note, when the level at point 1 is increased beyond 1 volt it is beyond the logging range of the amplifier. Similarly, if the input level is decreased 10 dB below the nominal minimum input level, the output increment is different. A curve of the ends of the logging range is shown in Fig. 5-11.

From the VR circuits, the signal is applied to input preamplifier Q3105 in the Log Amplifier circuits through coaxial connector P621. The input preamplifier provides transfer from 50 Ω input to the high impedance input of the 1st amplifier stage. The input signal is also applied to transistor Q2105, a common-base amplifier, that acts as a buffer to supply the 10 MHz IF signal to the rear panel connector.

From the input preamplifier, the signal is applied to the first of seven cascaded amplifiers that consist of Q3100/Q1095, Q3090/Q1080, Q3075/Q1070, Q3055/Q1050, Q3045/Q1035, Q3030/Q1025, and Q3015/Q6010, plus the associated circuitry. These stages are similar, except that
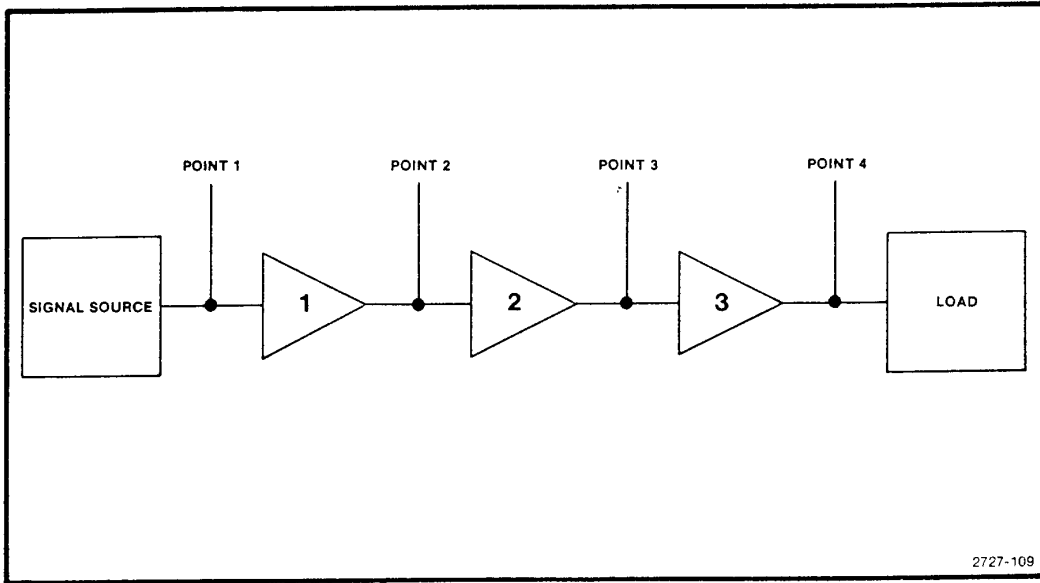
Fig. 5-9. Three-stage log amplifier.
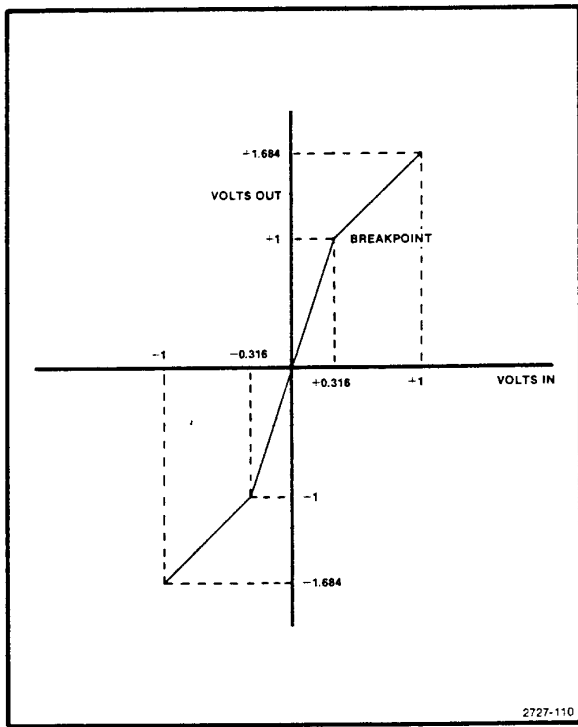
Fig. 5-10. Log amplifier gain curve showing breakpoint.

the first three contain an extra set of diodes for a second gain step. The following description of the last stage is typical. The second step gain change in the first three stages is described afterward.
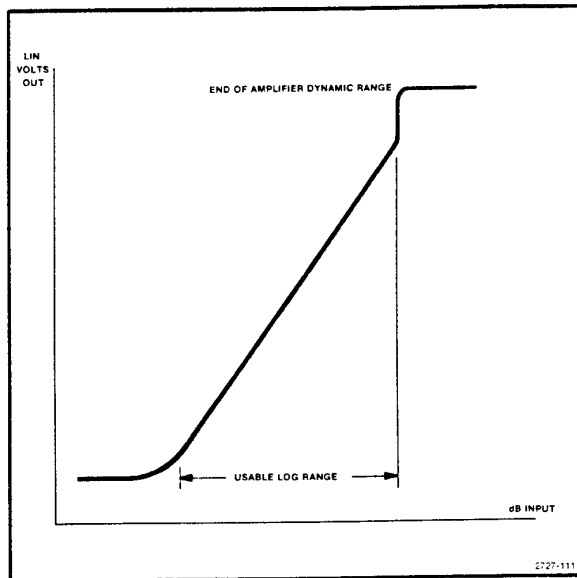
Fig. 5-11. Ends of logging range.

When the input level to transistor Q3015 is less than approximately 60 millivolts peak-to-peak, the transistor conducts enough to maintain forward bias on both series limiting diodes, CR4015 and CR4012. The RF signal path at that level is through the diodes, capacitor C5014, and resistors R4010H, R4010B, R4015, and R4010D, to common-base amplifier Q6010. The gain of the stage is approximately 10 dB under these conditions. As the input

signal voltage increases, more current flows through CR4015, to increase the reverse bias of CR4012. This sharply reduces the stage gain to unity. The signal current then flows only in R4010B, R4015, and R4010D. This change takes place during the positive-going portion of each cycle. The opposite occurs during the negative-going portion of the signal above the minimum input level. As the input signal increases beyond the point at which the gain of the final stage decreases to unity, the same sequence occurs in the preceding stage, Q3030/Q1025, and so on in succession, back to the first stage, Q3100/Q1095.

Signal levels above this point activate the second tier of gain reduction in the first three stages. Each stage incorporates a second set of diodes that reduces the gain by another 7 dB. In the first tier of gain reduction, reduction started at the last stage and proceeded to the first; in the second tier, the reduction starts at the first stage and proceeds to the third.

In the first stage, diodes CR3089 and CR2087, are forward biased when the stage is in the unity gain mode. Limiting occurs in the same manner as described above with a further increase in input signal level, and results in less than unity gain through the stage (approximately 1/3). The one, two, three reduction sequence is established by the values of pull-down resistors R3082, R2076, and R2066.

Detector Circuit

The Detector circuit detects and filters the Log Amplifier circuit output signal and produces the VIDEO signal that is transmitted to the Video Amplifier circuits. The circuit consists of an operational amplifier with a diode detector in the feedback path and a low-pass filter at the output.

Actually, the circuit called an operational amplifier is not easily recognized as such. It is made up of grounded emitter amplifier Q4025 and a differential amplifier consisting of Q4030 and Q4035. The summing node for the negative input is the base of Q4025 (the positive input is at the grounded emitter of Q4025). Also, the differential amplifier is designed for high impedance output to allow the current that is available from Q4025 to drive the operational amplifier very rapidly during the period when both detector diodes (CR5033 and CR5027) are effectively open circuited; that is, when the output is near 0 volt. When neither diode is conducting, it is necessary that the output change rapidly through that zone. Note that the network consisting of resistors R5032, R5029, R5020, and capacitor C5029 is included to stabilize the dc operating point.

Figure 5-12 shows a simplified schematic diagram of the detector circuit. As shown in this diagram, two detector diodes (CR5033 and CR5027) are used, but only the positive half cycle is taken as the output (from CR5027). The output from the collector of transistor Q4035 is applied to the diodes through capacitor C5035. Ac coupling is used on both sides of the detector to prevent temperature coefficient effects of the operational amplifier from affecting the detector output. This isolation provides that the detector charges and discharges capacitors C5035 and C5024 by the current induced in each half cycle of the signal without changing voltage level.

This detector operates as an area (average) detector despite the fact that the Log Amplifier circuits operate on peak principles. It is possible to use an average detector because of some very selective tailoring in the Log Amplifier circuits. For instance, resistor example R5021 in the final log amplifier stage is sized to reduce the amount of current standing in the final stage output diodes, thus tapering the curve very slightly to improve linearity at the lower end of the curve. Log Gain adjustment R4020, in the final amplifier stage, is adjusted for increased linearity at the top of the curve.

As shown in the diagram, the positive-going output signal, from the detector, is applied through a low-pass filter consisting of capacitors C7024, C7014, C7021, C7011, and inductors L6011, L8021, to the Video Amplifier.

$\langle\!\langle 6 \rangle\!\rangle$

DISPLAY SECTION

FUNCTIONAL DESCRIPTION

The display section performs several functions:

1) it accepts the VIDEO signal from the IF section, and processes the signal, and provides the vertical crt plate drive signals;

2) it processes the sweep voltages from the sweep section and produces the horizontal crt plate drive voltage. (If Option 02, Digital Storage is included in the instrument, vertical and horizontal signals are further processed by that circuit group;)

3) it accepts character information from the instrument data bus and generates crt plate drive signals to display alpha and numeric characters;

4) it accepts control levels from front panel beam controls and generates unblanking signals to control display presence, brightness, and focus.

Video signals from the IF section are applied to the Video Amplifier. In the logarithmic mode, the signal is amplified
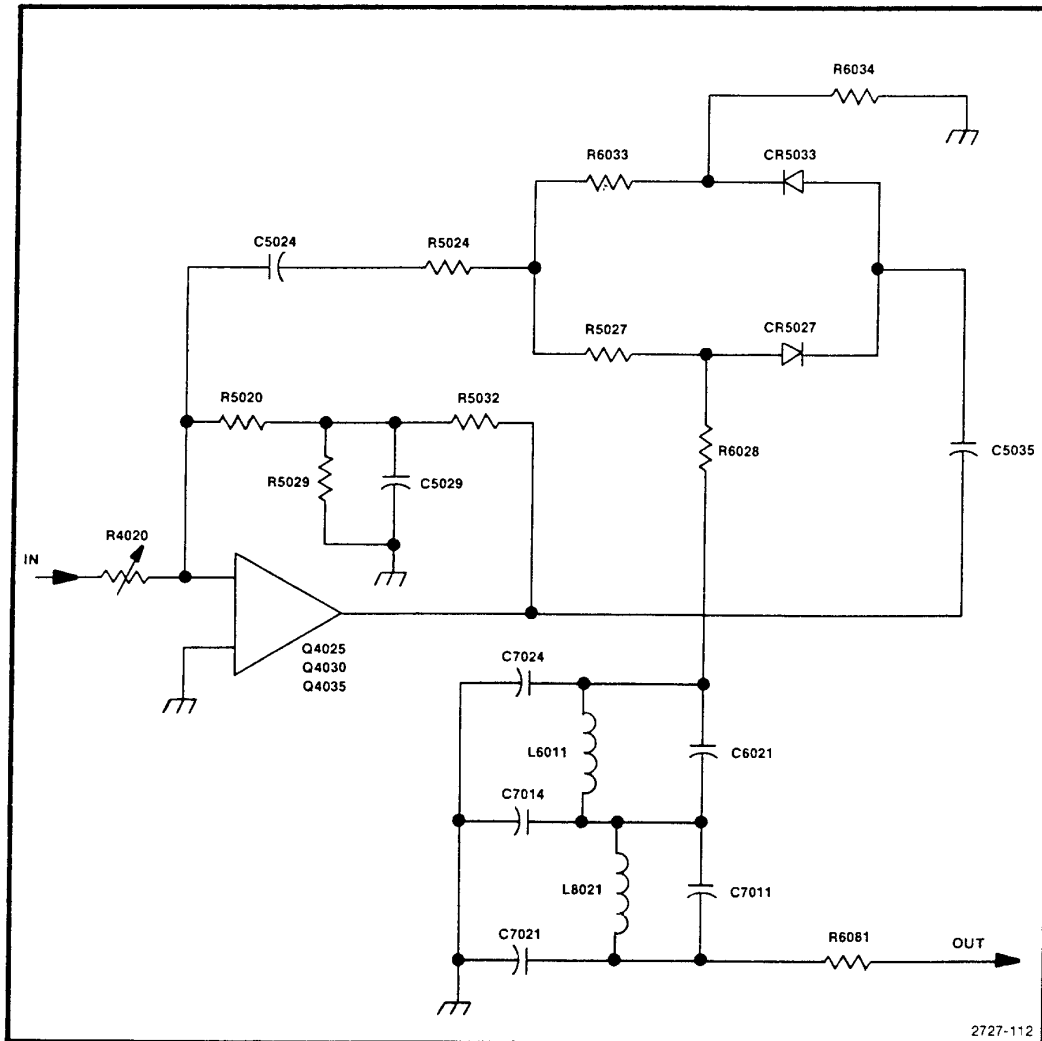
Fig. 5-12. Simplified detector circuit.

linearly and applied to the Video Processor. In the linear mode, amplification is exponential to convert the logarithmic characteristic to linear function. In either mode baseline compensation, from the Video Processor, is applied to the video signal to compensate for any unflatness in the front-end response. Also at the output of the Video Amplifier, a pulse stretch circuit alters narrow pulses so data can be displayed by the Digital Storage logic in instruments that include Option 02.

From the Video Amplifier, the output is applied to the Video Processor. Three functions are performed by the Video Processor. The first is unflatness compensation for front-end response variations. Video filtering, the second function performed by this circuit block, allows for selection of six video bandwidths (30 kHz, 3 kHz, 300 Hz, 30 Hz, 3 Hz, and

0.3 Hz) under control of the instrument microcomputer. The third function is out-of-band blanking. This blanks the upper and lower ends of the local oscillator swept frequency range to provide a selected window for the display. This is also controlled by the microcomputer.

In instruments equipped with Option 02, the Digital Storage logic provides operator selection of various display modes for observing the signals from the Video Processor. These modes are: MAX HOLD, SAVE A, B—SAVE A, VIEW A, and VIEW B and signal averaging or peak level display. The circuit block consists basically of:

1) vertical circuits that digitize signals at 512 points across the display and store those digitized data for display or processing, and

2) horizontal circuits that translate the sweep signal into memory address into which the signal data are stored. The stored signals are then used for the various processing as required by operator display selection, and for recreation of the display. From the Digital Storage logic, horizontal and vertical signals for the recreated displays are applied to the Deflection Amplifiers.

The Deflection Amplifiers receive vertical signals from the Digital Storage (in Option 02 instruments), or the Video Processor, and sweep voltage from the Sweep section, along with readout data from the Crt Readout circuits and produce signals to drive the crt for the display. In Option 02 instruments, the Digital Storage or Video Processor vertical outputs may be selected. In non-Option 02 instruments, the Video Processor output is displayed. Likewise, horizontal signals from either the Digital Storage logic or the Sweep section can be selected. During the display segments in which digital crt readout is required, the Deflection Amplifiers input signals are supplied by the Crt Readout logic. The amplifier contains the switching circuits to perform the above selection functions, and amplifier stages to produce the plate drive signals.

Crt readout data is controlled by the Crt Readout logic. These circuits generate letters and numbers for display under control of the microcomputer. Using data received from the data bus, a character memory and generator circuit derives each character. Digital signals, describing each character, are then translated into deflection signals by digital-to-analog converters. These signals are applied to the switching logic in the Deflection Amplifiers.

Beam intensity, nominally from the front panel, is implemented in the Z-Axis logic. Unblanking for display of either signals or readout data, and baseline clipping is also implemented in the Z-Axis logic. Control of unblanking is by signals from the Sweep section, the Crt Readout logic, the Deflection Amplifiers, and the Digital Storage logic.

VIDEO AMPLIFIER ⟨22⟩

Refer to the block diagram adjacent to Diagram 22. The Video Amplifier circuits provide for the selection of either logarithmic or linear display mode, for the selection of dB per division in logarithmic mode, for selection of pulse stretching in narrow peak signal operations, and for offsetting the signal amplitude during the signal identify mode. These circuits consist of the log mode amplification and dB/div switching circuits, the linear mode amplification and gain control circuits, the pulse stretch circuit, and the various digital control circuits.

Log Mode Circuits

The Log Mode circuits accept the VIDEO signal from the Log Amplifier and process that signal to add offset for selecting the segment of the log amplifier gain curve to be displayed. It also allows for selection, under program control in the 492P, of display gain steps of 1 to 15 dB per division on the screen. (Only 2 dB and 10 dB/Div are selectable from the front panel. The 492P can select all steps under program control.)

The signal from the Log Amplifier is applied to preamplifier U4090A. The VIDEO 1 signal from the Video Processor is also applied to U4090A. This signal compensates for flatness errors in the front-end circuits by offsetting the VIDEO signal in the opposite direction equal to the unflatness. The two signals are summed at the input of U4090B with the reference level set by Input Reference Level potentiometer R4071 (this reference level will be described later) and with the output from digital-to-analog converter U5041.

Converter U5041 converts the microcomputer commands to an offset signal which selects that portion of the Log Amplifier curve on which to place the display. The concept for this offset is as follows (refer to Fig. 5-13).
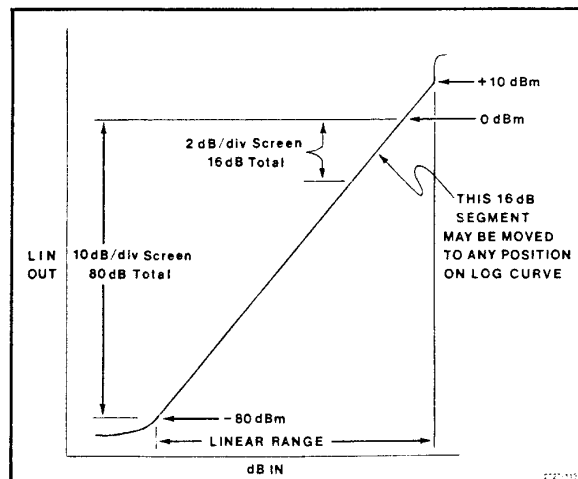

Fig. 5-13. Selection of display position on log scale.

If the display is in dB/div, changing the POSITION control, which is located after the log amplifier, is the same as changing the signal level, or gain, before the log amplifier. Thus, instead of using a large amount of linear gain change

before the log amplifier, a digital-to-analog converter is used to effectively move the display up or down the log curve. This process is called "offset" and it accomplishes the same effect as moving the POSITION control, except that the display on screen does not change, only the signal level required to reach the reference level changes.

Since the non-programmable 492 allows selection of either 10 dB per division or 2 dB per division, and the programmable 492P allows selection of 1 to 15 dB per division, the system must allow the gain to change while keeping the top of the screen constant, and must allow any 16 dB segment (in 2 dB/div mode) to be displayed. Nominally, the Log Amplifier operates with 0 dB or at the top of the screen.

The output of preamplifier U4090A is equivalent to 20 mV/dB. Full screen is always 2.2 V. At 2.2 V, the output of variable gain log amplifier U4090B is 0 volt, the only voltage at which the resistors in the switching network in the feedback circuit of preamplifier U4090B can be switched without changing the output voltage. (The switching network will be described later.) The 2.2 volt output of U4090A is adjusted during calibration to full screen by Input Ref Lvl (input reference level) potentiometer R4071.

From U4090B, the output signal is applied through FET Q5090 (if that transistor has been turned on by data bit 6 when 6 is high or a 1) to output operational amplifier U4090C, then through emitter follower Q4100 to the Video Processor via the front panel LOG CAL potentiometer. The Output Ref Lvl (output reference level) potentiometer, R4081 in the input circuit to U4090C, is used to adjust the output to provide a full screen display after Input Reference Level potentiometer R4071 is set for no change in the output of U4090B when switching from 10 to 2 dB or vice versa.

As an aid to understanding the system operation, it is probably useful to understand the basic calibration sequence that includes the above two controls. The sequence is as follows:

1) the digital-to-analog converter output voltage is calibrated by adjusting the front panel AMPL CAL control so that the output is appropriate for 10 dB per division;

2) the Log Amplifier detector circuit gain is adjusted so the Log Amplifier output agrees with the digital-to-analog converter output;

3) input Ref Lvl potentiometer R4071, is adjusted for no change in output level from U4090B when alternately pressing the 10 dB and 2 dB selector switches on the front panel;

4) output Reference Level potentiometer R4081 is adjusted for a full screen display.

The gain switching network provides for switching 15 resistance values into the feedback path of variable gain log amplifier U4090B, and consists of four FET switches (Q4075, Q4070, Q5070, and Q5075) and four resistors (R7071, R6074, R6073, and R6082). The FET switches, controlled by data bits 0, 1, 2, and 3 from the analyzer data bus; connect feedback resistors for U4090B in 15 value combinations as determined by the binary content of the four data bits.

In the non-programmable 492, only the 10 dB per division and the 2 dB per division selections are available and are controlled by front panel switches through the analyzer microcomputer. In the programmable 492P, the full 15 combinations are selectable through program control.

Linear Mode Circuits

The Linear Mode circuits accept the output from log preamplifier U4090A and rescale the signal level to linear values. Since no switching is provided in the Log Amplifier (that is, all signals are logarithmically scaled), to operate the system in linear mode requires that the signal level be re-exponentiated. Thus, high gain is required at the top of the screen and low gain is required at the bottom of the screen to offset the characteristics of the Log Amplifier.

In addition to the signal path described in the Log Mode circuits, the output from preamplifier U4090A is also applied to linear mode amplifier U4090D, an operational amplifier with a successive resistor network in the feedback path. From this amplifier, the output signal is applied through FET Q5090 (if that transistor has been turned on by data bit 5 from the analyzer data bus being a 1) to the summing node at the input to output amplifier U4090C. After this point, the signal path is as described in the Log Mode circuits description.

Starting at the signal level that represents the top of the screen (0 volt) at the output of linear mode amplifier U4090D, the operation of the network is as follows.

With a 0 dBm input from the Log Amplifier to the Video Amplifier, the output of U4090D is 0 volt. At that level, the feedback path is through only resistor R6104. The other feedback path resistors (R7097, R7096, R7092, and R7093) are not in the path because the switch transistors are biased off by the bias network consisting of resistors R7082, R7081, R6085, R7086, and R7095, plus diode CR7095. (The diode is included for temperature compensation purposes.) As the display moves away from full screen, the output of U4090D rises positive and transistor Q6115 is biased on, thereby placing R7097 in parallel with R6104 and reducing the gain of U4090D. Further increases in the out-

put of U4090D cause transistors Q6110, Q6090, and Q6095 to conduct in sequence and add resistors R7096, R7092, and R7093, respectively, in parallel to the feedback path. The sequential adding of resistors into the feedback path effectively reduces the gain of U4090D exponentially. Although it may appear that such a system would result in steps of gain resolution, the reaction characteristics of the transistors smooth the transitions and result in a smooth exponential gain curve.

Pulse Stretcher Circuit

The Pulse Stretch circuit, under control of the analyzer microcomputer widens narrow peak signals to allow the Digital Storage circuit time to acquire such signals. If this is not done, the 9-microsecond digitizing rate of the Digital Storage circuits is too short to acquire very narrow signals. The circuits accomplish this function by stretching the fall time of fast pulse signals. The circuit consists of FET switch Q7110 and the associated components in the feedback path of the output operational amplifier U4090C.

When pulse stretch mode is not selected (by data bit 7 from the analyzer data bus being a 0), FET switch Q7110 is off. With Q7110 off, capacitor C7104 is not in the circuit and the normal feedback path for U4090C and extra pulldown current is provided through resistor R5108. This allows the U4090C output to fall as fast as it rises.

When pulse stretch mode is selected (by data bit 7 being a 1), FET switch Q7110 is turned on and capacitor C7104 is inserted into the feedback circuit to slow the fall of the output. Also, the only pulldown current is through resistor R5086. Diode CR7101 serves only to isolate the pulse stretch circuit from the output circuit of the output amplifier. Diode CR5101 turns on at low levels to prevent the amplifier output from going too far negative and slowing the response when the input changes. When the output of Q4100 swings positive, the diode CR5101 disconnects. The primary advantage of this circuit is that the operational amplifier removes offsets by controlling very closely the voltage at the emitter of Q4100.

The Identify circuit permits the operator to check displayed signals as true or spurious. This feature is implemented elsewhere in the analyzer, except for an offset that is applied in the Video Amplifier. The test is accomplished by changing the frequencies of the 1st LO and the 2nd LO an equal and opposite amount related to the harmonic number used. If the signal is true, it will not move. As a check, the display baseline of the signal that results from the frequency is shifted about one division so the alternate display is right below the other display.

Thus, if the display is two similar signals separated in amplitude, the signal is true. This offset is inserted from the analyzer data bus through latch U6050 and buffer U6060 to the summing node of the output amplifier U4090C.

Digital Control Circuit

The Digital Control circuit provides the control signals for selection of the various Video Amplifier functions and consists of address decoding, data latching, and buffering circuits. From the analyzer data bus, address data and the DATA VALID signal are applied to the address decoder U6070 through edge connector pins 30, 26, 25, 27, 28, and 31. The decoder produces two enable signals that are applied through inverter U5070 to gain latch U6040 and mode latch U6050.

The Gain latch IC U6040, is an eight-bit latch that supplies command data to eight-bit digital-to-analog converter U5041 to offset the Log Amplifier output signal. Mode latch U6050 is an eight-bit latch that supplies command data through buffer U6060 to select the resistors in the dB per division switching circuit and to select identify, pulse stretch, and log or linear mode.

VIDEO PROCESSOR ◇23◇

Refer to the block diagram adjacent to Diagram 23. The Video Processor circuits perform band leveling, video filtering, and blanking. The circuits that perform these functions are described in the following paragraphs.

Video Leveler Circuits

Video leveling compensates for those characteristics of the analyzer front-end microwave circuits that cause unflat response in band 4 (5.4 to 18 GHz). Since band 4 is a multiplied band, any unflatness is accentuated. This leveling is accomplished through a programmable perturbation of the display baseline that is opposite in direction from the flatness error in the front-end circuits. As analyzer signal power output decreases, the baseline rises an equal amount in compensation; or, as power output increases, the baseline falls an equal amount. The perturbation signal is actually produced by a normalizer integrated circuit that produces 19 evenly spaced values of the input voltage, but with each value corrected to compensate for unflatness.

The PRESELECTOR DRIVE signal from the 1st LO Driver circuits, is applied through edge connector pin 54 to an input translation circuit that consists of two current drivers (U3045A and half of Q3038, plus U3045B and the other half of Q3038). Since the PRESELECTOR DRIVE signal is directly related in amplitude to displayed analyzer frequency, the nominal +10 V to −10 V excursion voltage versus frequency curve in maximum span, relates to the full bandwidth. This 20 volt maximum excursion is scaled to a

precise current that ranges from 1 mA at +10 V to 0 current at −10 V for application to the normalizer IC to generate the baseline perturbation signal. Actual signal scaling is done by the U3045A/Q3038 current driver. The output signal is applied to the normalizer SWP IN input, pin 5. The second current driver, U3045B/Q3038, generates a 2 mA reference current for the normalizer. Horizontal Freq adjustment R1069 in the input translation circuits allows for shifting the 19 evenly spaced points up or down in frequency for compensation flexibility.

Normalizer IC U2039 operates as a shaper and contains 19 bi-polar transistors that turn on then off in a sequence as the current input to pin 5 decreases from 1 mA to 0 mA. The collector of each of these IC transistors is connected to a potentiometer that allows for output trimming as shown on Diagram 23. Potentiometer R1061 is active with no current; R1013 is active at 1 mA. The trimming operation will be described later in these paragraphs.

From the normalizer, the output is applied through a jumper switch to buffer amplifier U2055B, which has a gain of five, then to offset amplifier U2055A. This amplifier has a gain of two, but its primary purpose is to offset the 0 to +5 V (normal); 0 to −5 V (invert) buffer output to the levels required by the Log Amp circuits. The range required by the Log Amp is −5 V (min). The output voltage is a series of linear interpolations of the voltage between adjacent trimming resistors at the outputs of the normalizer. Compensation adjustment R1065 allows for setting correct interpolation.

Jumper switch P2060 selects the input side of buffer amplifier U2055B. This provides the means to invert the buffer output. During calibration, the procedure is as follows: Leveler Disable jumper P3035 is removed, a test signal with a normal uncorrected baseline waveform is displayed and stored, the Mode jumper (P2060) is removed and reinstalled in the invert position, the disabled jumper is reinstalled, the stored waveform is displayed with the normalizer output waveform superimposed, and the 19 potentiometers are adjusted for exact compensation. The Mode jumper is then removed and reinstalled in the normal mode position. Thus, the output on the Video 1 line is opposite in polarity and equal in amplitude to the undesired variations.

As stated previously, significant compensation is required only on band 4. Selection of band 4 is indicated by data bit 0 switching to a 1 (see the leveling table at the top right corner of Diagram 23). When DB0 is a 1, pins 3 and 2 of switch U2015 are connected and the output from the offset amplifier (U2055A) is supplied out as the VIDEO 1 signal at edge connector pin 49.

Minor compensation is required for band 1 only when preselection is specified (Option 01). With Option 01, a minor slope caused by the 1.8 GHz lowpass filter and 2 GHz limiter is corrected by adding two resistors in series between the PRESELECTOR DRIVE signal input and the VIDEO 1 output signal. These two resistors, R4023 and R3026 (note that R4023 is selected at factory calibration), form a voltage divider with R4046 and are inserted by connecting pins 6 and 7 of switch U3025. This switch is controlled by inverter Q4025, which is, in turn, activated by data bit 6 being a 0. As shown in the VIDEO BLANKING table on Diagram 23, data bit 6 is a 1 except when Option 01 is selected.

Video Filter Circuits

Video filtering provides selection of one of six bandwidths, under the control of the analyzer microcomputer. As shown in the VIDEO FILTER table on Diagram 23, data bits 1 through 4 select any of six bandwidths: 30 kHz, 3 kHz, 300 Hz, 30 Hz, 3 Hz, and 0.3 Hz. Either wide or narrow-band filtering is selected at the front panel (30 kHz, 3 kHz, and 300 Hz are defined as wide-band; 30 Hz, 3 Hz, and 0.3 Hz are defined as narrow-band), and the microcomputer makes the selection, based on such factors as sweep rate and total dispersion. With no video filtering (all data bits equal 0), the video system bandwidth is 500 kHz, as determined by circuits that follow the Video Processor, which has an internal bandwidth of 3 MHz.

Two signal inputs can be applied to the Video Filter circuits: EXT VIDEO and INTL VIDEO. The EXT VIDEO signal, from the rear panel auxiliary connector, is applied to pin 15 of switch U3063 through edge connector pin 53. The INTL VIDEO signal from the Video Amplifier circuits (via the front panel LOG CAL control) is applied to pin 2 of switch U3063 through edge connector pin 51. Note that the two left sections of switch U3063 are normally held energized (pins 2 and 3 connected, pins 15 and 14 disconnected) by the +5 V supply through resistor R3064. If the EXT VIDEO SELECT line (also from the rear panel auxiliary connector through edge connector pin 55) is grounded, those switch sections are de-energized and the External Video signal is applied through, or around, the filter to become the VIDEO FILTER OUT signal at edge connector pin 57. This is shown in the simplified schematic diagram of Fig. 5-14.

As shown in the figure, when no filtering is selected (all data bits equal 0), either the internal or external signal is applied around the filter because the two right sections of switch U3063 are not energized by data bit 1. When data bit 1 is high (1), filtering of some value will be selected by bits 2, 3, and 4, which control three sections of switch U2015 to add or delete filter time constant.

Fig. 5-14. Video filter simplified schematic.

The filter consists of resistors R2023, R2021, R2022, and capacitors C3026, C2016, connected between two comparators (U3062 and U2066). Table 5-7 lists the components that are in the circuit for each of the six bandwidths. Note that data bits 2, 3, and 4 are applied to switch U2015 pins 8, 16, and 9, respectively, to select components.

From buffer U2066, the signal is applied through contacts 7 and 6 of switch U3063 and edge connector pin 57 as the Video Filter Out signal.

Table 5-7
FILTER COMPONENT COMBINATIONS

Bandwidth	DB = 1	R2023	C3026	R2021	R2022	C2016
30 kHz	1	X	X	X	X	
3 kHz	1,4	X	X	X		
300 Hz	1,3,4	X	X			
30 Hz	1,2	X	X	X	X	X
3 Hz	1,2,4	X	X		X	X
0.3 Hz	1,2,3,4	X	X			X

Video Blanking Circuits

The Video Blanking circuits allow for selective blanking of the lower and upper ends of the local oscillator range. This is required because the local oscillator sweeps full span mode regardless of the prescribed band limits. Thus, the video system is designed to effectively open a display window only during the time for display. Data bits 5, 6, and 7, under control of the microcomputer, select the appropriate amount of display for each band.

Since the video filtering is on the Video Processor board, and the PRESELECTOR DRIVE signal (which provides frequency information, in voltge form) is also available, this board is a logical place for video blanking. Switch U3063 incorporates a disable function that, when provided a low input, opens all switch sections regardless of individual section input. Using this feature, the Video Filter Out signal may easily be blanked at will.

Control for this disable function is from a combination of outputs from two comparators, U3015A and U3015B. Inputs to these comparators are from the PRESELECTOR DRIVE signal and a combination of voltage dividers that are switch selected under control of data bits 5, 6, and 7. The PRESELECTOR DRIVE signal is applied from edge connector pin 54 to the minus input side of U3015A through divider resistors R4013 and R4012, and to the plus input side of U3015B through divider resistors R4014 and R4011. These dividers reduce the $+10$ V to -10 V excursion of the drive signal to $+2.5$ to -2.5 V, the maximum input level to the comparators.

Input to the plus side of U3015A is from a divider that consists of resistors R3011, R3012, R4024, and R4015. Note that the excursion of R4024 is controlled by data bit 5 through pins 15 and 14 of switch U3025, and that the inclusion of R4015 is controlled by data bit 7 through pins 2 and 3 of the same switch. Thus the junction of divider resistors R3011 and R3012 may be connected to -10 V through R4024 or to ground through R4015. Refer to the VIDEO BLANKING table on Diagram 23 for data bit states for different bands.

Input to the minus side of U3015B is from a divider that consists of resistors R4018, R4017, and R3028. Note the inclusion of R3028 is controlled by data bit 6 through pins 10 and 11 of switch U3025. Adding resistor R3028 connects the junction of R4018 and R4017 to $+10$ V through R3028. This arrangement of switching negative and positive levels for comparison with the reduced PRESELECTOR DRIVE signal, enables the top and bottom extremes of the frequency excursion to be blanked by activating the disable function of switch U3063. This blanking is under the control of the microcomputer.

DIGITAL STORAGE ⟨24⟩ ⟨25⟩

The addition of Option 02 to the basic 492/492P provides the operator with the capability of selecting the method for displaying and processing information contained in the digital storage memories. This allows operations such as determining the highest amplitude that occurred during a selected period (MAX HOLD mode), storing a signal for later examination (SAVE A mode), subtracting one signal from another (B − SAVE A mode), averaging signals (AVERAGING mode), and comparing signals (VIEW A, VIEW B modes). Two memories are used independently in these operations to store two complete signals that are each digitized at 512 points across the sweep. Thus, two signals may be observed simultaneously or processed in various ways.

In MAX HOLD mode, the highest amplitude at each of the 1024 points in successive sweeps is stored and displayed. In SAVE A mode, a signal is stored in one memory for later examination, and is not updated. In the B − SAVE A mode, the A signal is stored and not updated, then arithmetically subtracted from the B signal, which is stored and continually updated. In the AVERAGING mode, the display area is divided by a horizontal cursor. Above the cursor, signals are peak detected and displayed; below the cursor signals are averaged. In the VIEW A and VIEW B modes, the contents of the selected memory or memories are displayed.

Graphical presentation of mathematic functions or experimental data is common today. One class of such graphs is those that have a single Y value for each X value. An alternate presentation of the data in this graph would be a table in which the X coordinate values were simply listed along with a corresponding Y value for each X value. In further simplification, if the first X value and the spacing between X values (assuming that all spacings are equal) were known, the two column table could be reduced to a single column with the X value implied by the position of the Y value in the column. This then is the essence of digital storage: to convert a vertical analog voltge (Y coordinate value) to a binary number and insert that number in a stored table. The location of the Y value in the table is determined by converting to binary the analog sweep voltage (X coordinate value). Once the table is created by storing a set of binary numbers representing values across a waveform, the waveform can be recreated at any time by converting the table values (Y) and positions (X) back to analog voltages representing amplitude and sweep position.

The digital storage system used in the 492/492P uses two tables: A and B. Table B is always updated on every sweep. Table A is changed unless SAVE A mode is selected. There are 512 A values and 512 B values. The spacing between values is the same throughout both tables, but the

starting point for table B is shifted slightly so that when both tables are being read, the readout values are interlaced.

When the signals are recreated, the operator has the option of displaying either A or B, or both A and B. If both are to be displayed, and SAVE A mode is also selected, the contents of both table A and table B are drawn, each display in its own trace. If SAVE A mode is not selected, the contents of both table A and table B are displayed on one trace, with 1024 value positions across the screen. A third trace option is also available. In the B minus A mode, the displayed values are those resulting from an arithmetic operation and are the difference between the contents of table A and table B for each X value of analog sweep voltage.

Since a signal waveform is continuous and a table has discrete X values, an algorithm is used to determine the Y value to be stored for a particular X value. This allows the operator to select one of two methods for determining Y values: peak or average. The Y analog voltage is continuously sampled, with the sampling rate dependent upon sweep speed. For each X value, there are always at least two samples and there may be as many as 2^{17} samples. From this set of samples then, the user may select either the largest sample value (peak value) or the mean of all the samples (average value). Selection between peak and average is controlled by the front panel PEAK/AVERAGE control, which sets a dc level that is compared with the analog vertical input to produce the PEAK/AVERAGE logic signal. When the input signal is below the level selected by the front panel control, the signal is averaged; when the input is above that level, the peak signal is displayed. The dc level appears on the display as a positionable horizontal line. This marker line is created by switching the dc level to the analog output line during the marker cycle to produce the MARKER logic control signal.

Superimposed on the marker line is an intensified spot called the UPDATE MARKER, which indicates the X value at which new Y values are being computed for display update. The update marker is formed by comparing the analog sweep input to the display analog X output. When the two are the same value, the sweep is forced to pause, thus increasing the marker intensity at that point. Refer to the block diagrams, adjacent to Diagrams 24 and 25.

Central to the 492/492P digital storage system are two specially designed and manufactured IC's; U1023 and U2032. Vertical section IC U1023 contains the vertical acquisition and display logic, and peak detection, signal averaging, Z-axis blanking, and special Y-value processing circuits. Horizontal section IC U2032 contains the horizontal acquisition address counter, horizontal display counter, 10-bit RAM address multiplexer, and a programmable logic array system control matrix. The remainder of the digital storage control circuits consists of two 8-bit digital-to-ana-

log converters, two 10-bit digital-to-analog converters, one 10-bit latch, 8k bits of random access memory, and various ancillary circuits. Timing is controlled by clock pulses from the microcomputer board to pin 1 at approximately a 1 MHz rate. The two primary IC's, U1023 and U2032, are described as appropriate at the beginning of the vertical and horizontal section detailed descriptions that follow.

Vertical Section ⟨24⟩

Vertical Control. (Refer to Fig. 5-15.) The vertical analog voltage is converted to a Y binary value using an 8-bit successive approximation register. Nine clock cycles are required for each Y conversion. After the conversion has taken place, the successive approximation register produces the negative-going $\overline{SYNC}$ signal. Most functions on both the vertical and horizontal control IC's are synchronized by this signal. On the negative-going transition of $\overline{SYNC}$, the successive approximation register is reset to 10 00 00 00 (binary) and the next conversion cycle begins. Incoming data bits are latched into the successive approximation register on the negative-going clock transition. From the register, the output data are applied to the peak and the averaging circuits.

The averaging circuit consists of three groups of circuits: those that accumulate the grand total of all of the Y values for a given X value (this total is called the numerator), those that count the number of samples that make up the numerator (this total is called the denominator), and those that subtract and shift to perform the division process.

As each new Y value is converted, it is added to the eight least significant bits of the numerator. Each carry from the most significant bit of this addition is counted by a 17-bit ripple counter. The contents of this counter and the 8-bit sum are cascaded to form a 25-bit grand total. Each time a new sample is added to the numerator, a second 17-bit ripple counter is incremented to produce the denominator.

A division cycle is initiated when the horizontal control IC U2032, located on Diagram 25, detects a change in the X value. At that time, U2032 produces the ST DIV (start divide) signal. Upon receipt of this signal, and in synchronization with the $\overline{SYNC}$ signal, vertical control IC U1023 performs several functions (refer to Fig. 5-15):

1) it latches the current numerator in a 25-bit latch (25 to 1 data concentrator in the block diagram), and latches the denominator in a 17-bit latch (17 to 1 data concentrator in the block diagram);

2) it clears the numerator adder circuits (25-bit summation register in the block diagram);

3) it performs a 17-bit priority encode on the denominator and loads a 1 in the appropriate cell of the 25-bit shift register;
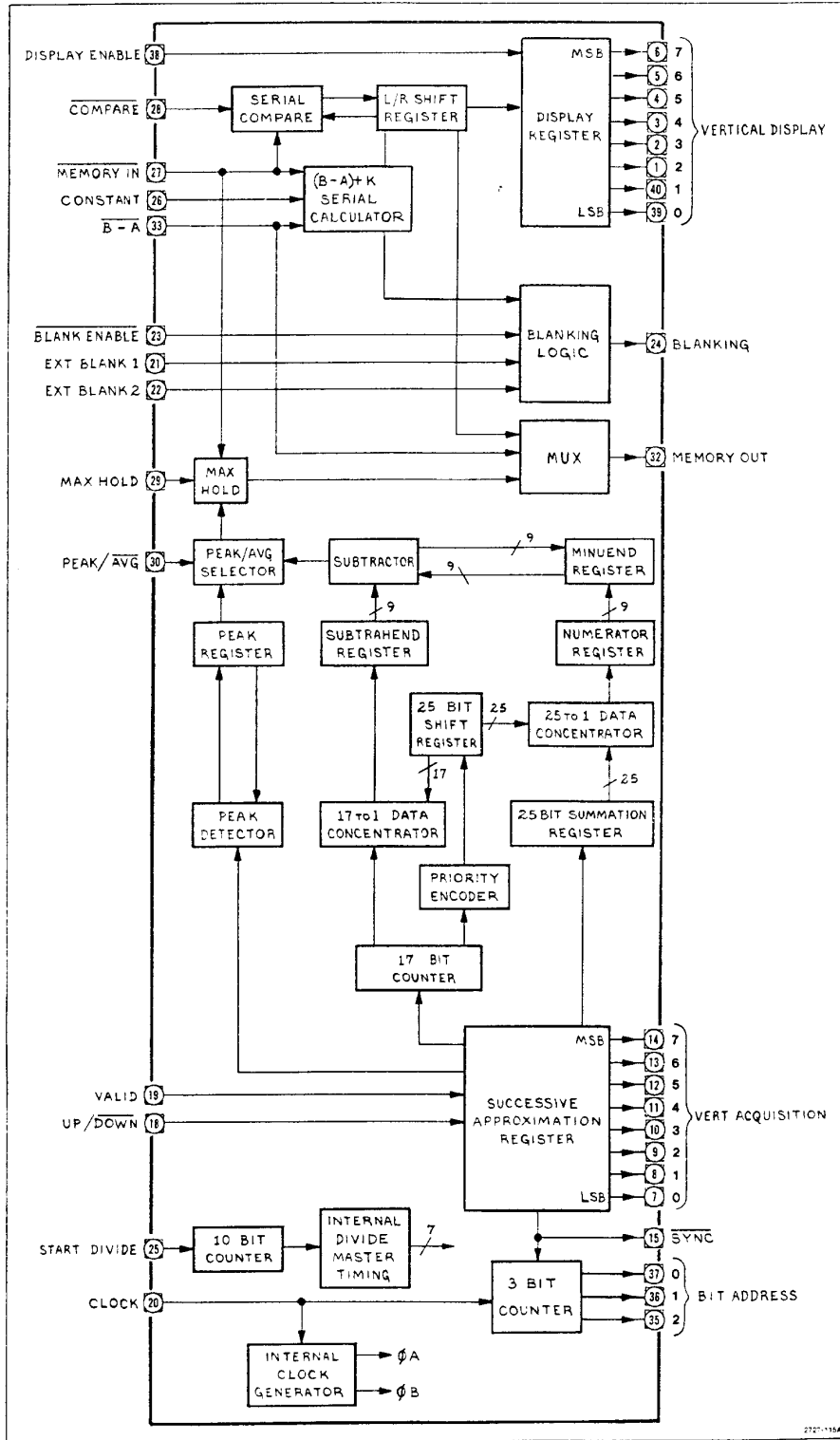
Fig. 5-15. Vertical control IC U1023 block diagram.

4) it loads the latched numerator and denominator serially into the divide circuit (subtractor in the block diagram) using the contents of the 25-bit shift register as a mask;

5) it clears the denominator ripple counter (17-bit counter in the block diagram) to zero.

Ten clock periods are required to load the numerator and denominator into the divide circuit. The cycle starts on a $\overline{\text{SYNC}}$ pulse and the first bit of the quotient is available shortly after the first clock pulse following the next $\overline{\text{SYNC}}$ pulse. Division is performed by repeated subtract and shift operations. The quotient is arrived at serially with the most significant bit first. Only 8-bit accuracy is required, so, by using the priority encoder output as a mask, the divider circuit is loaded with the 8 most significant bits of the denominator and the 16 most significant bits of the numerator. (Ripple borrow for a 17 by 25-bit subtractor would be so long as to be impractical.)

The peak circuit consists of a peak detector and an 8-bit peak shift register. In operation, the previous peak Y value from the last set of samples is still stored in the peak shift register at the start of a conversion cycle. At that time, the peak detector, which is a serial compare circuit, is set to the state that will question whether the old or new number is larger. Each bit of the new value is then compared with the corresponding bit of the old value, most significant bit first. When one value is found to be larger, a flip-flop is set and the smaller number is gated out of the shift register. The start divide logic signal being true then forces the peak detector to select the new value and ignore the number in the shift register.

The peak/average selector, a multiplexer, selects either the peak or average value to be routed to the memories under control of the PEAK/$\overline{\text{AVG}}$ signal. The selector output is routed through the max hold circuit, which functions in the same manner as the peak detector. When the MAX HOLD signal is high, the value that is routed to the output multiplexer is the larger of two values: the current memory value at the subject X coordinate or the previously selected peak or average value.

Timing for setting up the divide operation and clearing the numerator, denominator, and peak circuit is controlled by a 10-stage Johnson counter. NOR-gate taps are taken from appropriate stages to develop the necessary clear and latch timing pulses. Because the denominator is loaded into the divide circuit using a priority encoder, the most significant bit is always a 1. Space and power were saved by modifying the subtractor and not storing this 1.

All data enter and leave the memory serially. Data read from memory enter an 8-bit shift register, and timed by

$\overline{\text{SYNC}}$, are transferred to the vertical display output latch (display register on the block diagram). The same shift register is used for other purposes, so the DISPLAY ENABLE signal prevents non-display information from being transferred to the output latches. An example of data moving through this shift register is that during the B minus A display mode. The A value is first read from memory and stored in the shift register. As the B value is read, the subtraction is done serially and the answer is applied to the shift register. Since the subtraction must be performed least significant bit first, a set of exclusive-OR gates change the order of extracting B from memory. The direction of shift for the shift register is reversed also to present the most significant bit to the proper display latch. The shift register output is also applied to the output multiplexer.

In the subtraction, the operation performed by the serial calculator is not merely B minus A. The actual expression implemented is $(B-A) + K$, where K is a serial input external constant specified by the user. This permits zero to be placed anywhere on the screen. To avoid confusion, when $(B-A) + K$ results in an off-screen position, the subtractor blanks the display. This is done by examining the carry bit and borrow bit when the most significant bit is calculated. If either bit is a 1, the screen is blanked.

When SAVE A mode is not selected and both A and B are being displayed, maximum resolution is obtained (1024 points across the display). If this display includes a very narrow pulse, it is possible that the top of the pulse is only as wide as a single X coordinate (2 to 2^{17} samples). If this maximum value were in the B table and SAVE A mode were selected and B turned off, there would be an apparent drop in amplitude. For this reason, when SAVE A mode is selected, a special set of circuits in U1023 compares all A and B values that have the same X value and stores the larger in table A. This is accomplished by first reading the B value and storing it in the display shift register. Then, as the A value is read, it is compared with the B value and the larger of the two is loaded into the display shift register. Finally, the number in the shift register is written into memory from the shift register. This operation is performed once each time that SAVE A mode is selected.

Vertical control IC U1023 also contains a 3-bit synchronous counter that identifies the specific bit of an 8-bit vertical value that is to be read from memory or written into memory. This is the only memory addressing that is performed by the vertical control IC. All other addressing is under control of the horizontal control IC (U2032).

Digitizing Circuits. The input vertical signal, VID FLTR OUT, coupled through edge connector pin 60 is applied through buffer U2033 to sample and hold switch U1033, which is controlled by flip-flop U1011B. Flip-flop U1011B generates the sample pulse and is enabled during the clock

cycle after the last sample as indicated by the least signifi-cant bit from the successive approximation register in U1023. The switched sample is then applied through buffer U2032 to a summing junction, at which point the output current from the digital-to-analog converter (U2024) that is supplied from the successive approximation register is sub-tracted from the sample current, and the difference current is applied through comparator U1031B to pin 18 of U1023 as the UP/$\overline{\text{DOWN}}$ signal. Thus, the combination of the successive approximation register, the digital-to-analog converter, and the sample and hold circuit effectively pro-duces the binary equivalent of the input sample.

Address Decoding. The address decode logic accepts inputs from the address bus and produces the control sig-nals for read and write operations: $\overline{\text{CONT W}}$ (control write), $\overline{\text{DATA W}}$ (data write), and $\overline{\text{DATA R}}$ (data read). The control write signal is used to gate the control word from the data bus into control register U1022 to generate mode control signals. This control word consists of five bits that represent front-panel functions. If output Q6 is low, a peak operation is forced: if output Q6 is high and Q7 is low, an average operation is forced. The data read and data write signals are applied to the interface logic to control memory read and write operations.

Interface Logic. The interface logic in general performs control and interface functions between the active data cir-cuits in both the vertical and horizontal sections and the rest of the 492/492P. It allows the microcomputer to control the functions of the storage system and to access the digital storage memory, and it contains the circuitry for serial-to-parallel and parallel-to-serial conversion. (The micro-computer uses parallel transfer; the digital storage memory uses serial transfer.) Shift register U2021 is used to read data from memory to the data bus. Register U1021 is used to store information from the data bus for transfer to mem-ory. Multiplexer U2016 performs the parallel-to-serial con-version and applies the data output to gate U2015B, which acts as a buffer to supply either the multiplexer output or the MEM OUT (memory output) signal from U1023 to the memory as the DSDI (digital storage data input) data train.

The interface circuit group at the lower right corner of the diagram is the handshaking logic that works with the hori-zontal control circuits for access to memory and for control of when to increment the memory address counter. In either a data read or data write operation (when the corresponding signal goes high), flip-flop U2014B is triggered, which in turn releases the BUS REQ (bus request) line, allowing that sig-nal to go high. This signals the horizontal control circuit that access to memory is required. When the horizontal circuits recognize that request, those circuits pull the BUS REQ line low at the same time that SYNC is low. The interface logic detects the BUS REQ and SYNC low condition through U1013A, U1013B, U2011A, and U2012C, and produces the low $\overline{\text{BUS GRANT}}$ signal to indicate access to memory. The

$\overline{\text{BUS GRANT}}$ signal then enables shift register U2021 to shift data from memory or enable register U1021 and multiplexer U2016 to shift data to memory as indicated by the $\overline{\text{DATA R}}$ and $\overline{\text{DATA W}}$ lines. At the end of a data read cycle, gates U1012B and U2023C produce the INCR ADRS (increment address) signal to increment the address register in the horizontal circuits.

Maximum Hold. As described previously, when MAX HOLD mode is selected, circuits in U1023 compare the bina-ry equivalent of the input signal for a given X value with the information in memory for that same X value and cause the larger of the two to be stored in memory. The control signal that initiates this action is produced from Q5 of control reg-ister U1022. In combination with the VALID signal from the horizontal circuits, this signal produces the MAX HOLD command to U1023 through buffer U2023E and gate U1025A.

Constant Circuit. As described previously, in the B mi-nus A operation, a constant is used. This constant is inter-nally selectable with switch S1014. This switch, in combination with multiplexer U1015, supplies the constant to U1023. Multiplexer U1015 is in turn controlled by address bits 0, 1, and 2 to provide the proper switch signal to U1023.

Output Circuits. From the U1023 vertical display regis-ter, the parallel data output is applied to 8-bit digital-to-ana-log converter U1024. The converter output is then applied through a vector generator, consisting of an integrator (U1032 and C1031) with an associated feedback loop sam-ple and hold circuit, to the output storage/cursor switch. Integrator U1032 has a time constant that provides a ramp lasting between the existing sample and the new sample (that is, between sync pulses). Circuits U1033A and U1034 and capacitor C1038 make up a sample and hold circuit with U1034 acting as an output buffer. From U1034, the output current through resistor R1032 subtracts from the digital-to-analog converter output current to modify the slope of the output ramp. The output of the vector generator is then ap-plied to switch U1033B, which selects between the stored data and the marker under control of the buffered PEAK/AVG (peak/average) level control signal from U2034B and supplies the output to the horizontal circuits.

Peak/Average Level Circuits. The buffered PEAK/$\overline{\text{AVG}}$ signal is also supplied as a mode control signal to U1023 in combination with: the sample and hold up/down output from U2032, the VALID signal from the horizontal circuits, and Q7 of the control word from U1022 (always a 1), through buffer U1031A, gates U1025C, U1025D, U1025B, and in-verter U2023D.

Horizontal Section ⟨25⟩

A block diagram of the Horizontal control IC U2032 is illustrated in Fig. 5-16. The horizontal analog voltage is converted to a current table value through the use of a 10-bit tracking analog-to-digital converter, which consists of an up/down interlock and 10-bit up/down counter (U2032) and an external 10-bit digital-to-analog converter (U2036). As the sweep moves to the right, the counter increments; as the sweep retraces, the counter decrements. Each time the counter increments, a new X coordinate value is generated (the digital-to-analog converter output) and a ST DIV (start divide) signal is generated to start the storage cycle. The increment clock is the $\overline{SYNC}$ signal, the decrement clock is the basic 1 MHz clock divided by two. When SAVE A mode is selected, the counter skips every other binary number. Thus, only B coordinates appear as addresses.

Intelligence for the horizontal system is provided by a programmable logic array ROM state device (PLA). This PLA determines which trace is to be written on the screen, determines when to switch from read to write, generates the $\overline{B-A}$ coordination signals for vertical control IC U1023, controls the incrementing of the 9-bit display counter, and processes requests for the memory bus. Of these, the only function not obvious is the memory bus request. When an external device elects to read from or write to memory, it must request permission by allowing the BUS REQ (bus request) signal to go high. When that time becomes available, the PLA pulls the BUS REQ line low, signalling the start of a request cycle. For the next eight clock cycles, the multiplexer output lines are driven to the high impedance tristate mode.

The combination of the up/down interlock, 10-bit up/down register, 9-bit display counter, and horizontal display multiplexer constitute the primary circuits that:

1) convert the sweep voltage to binary form to generate X values to be written into memory, or

2) read the X values from memory by counting sync cycles and causing the external logic to read stored data from memory and produce a vertical signal (Y value) for each corresponding X value.

During acquisition cycles, the 10-bit up/down counter, controlled by the up/down interlock, operates in a loop with the external 10-bit digital-to-analog converter to derive the equivalent (X value) of a sample section of the sweep voltage. From the counter, the 10-bit output is applied to the 10-bit up/down register. During display cycles, the 9-bit display counter counts sync pulses to derive the X value. Either the 10-bit up/down register output or the display register output is applied to the horizontal multiplexer under control of the SELECT signal from the PLA. From the multiplexer, the output is applied to the memories.

Address Registers and Buffers. Address counting is accomplished by registers U2022, U2016, and U2012. These count INCR ADRS (increment address) pulses after having been reset to zero by the $\overline{CONT\ W}$ (control write) signal from the vertical section. From the address register, the outputs are applied to tristate buffers U1022 and U1016, which buffer the 10-bits of address from the counters and the DS R/$\overline{W}$ (digital storage read/write) signal line from the vertical section interface logic and multiplex those signals onto the HD (horizontal display) lines and R/$\overline{W}$ (read/write) line to the memories. These buffers are enabled only during the bus grant portion of the cycle for display of memory data. At all other times, horizontal control IC U2032 outputs control the HD lines to determine the memory address for update of memory data.

Tracking Analog-to-Digital Converter. As discussed previously, the 10-bit digital-to-analog converter operates as part of the loop that derives a binary equivalent of the SWP (sweep) input signal from the Sweep board. Converter U2036 accepts the output from the U2032 10-bit up/down counter and converts that output to an analog current that is subtracted from the sweep signal, which is applied at the edge connector pin 60 and through buffer U2044B. The result of this subtraction is then supplied to up comparator U2038A and down comparator U2038B, to produce the UP or DOWN signal, as appropriate to control the direction of the count of the 10-bit up/down counter in U2032. The counter then counts in the appropriate direction, thereby changing the digital-to-analog converter output to reflect the proper value. Overflow detector U1032 and underflow detector U1034 prevent the counter from counting too high or too low.

Update Marker Circuits. From U2032, the HD (horizontal display) signals are also applied to 10-bit latches U1024 and U1018. The outputs of these latches are applied to 10-bit digital-to-analog converter U2034. From the converter, the output current is applied through buffer U2044A, where it is converted to a voltage, to comparator U2042, which compares it with the sweep voltage and applies the output voltage to digital one-shot U1014A. The period of this one-shot is determined by counter U2024 under control of the low DISP ENBL (display enable) signal from the PLA in the horizontal control IC U2032. DISP ENBL, when high, indicates that valid data are to be transferred. Conversely, when DISP ENBL is low, the lack of valid data indicates retrace. One-shot U1014A produces the INTENSITY signal that is used to temporarily prevent counting by the 9-bit display counter in U2032, thereby effectively stopping the beam for a short time and causing a bright spot on the marker trace (cursor) to indicate the X point being updated. Also note that buffer U2044A also produces the HORIZ SIG (horizontal signal) that is sent to the Deflection Amplifiers.

Fast Retrace Blanking. Between the display of the B memory contents and display of the A memory contents, a
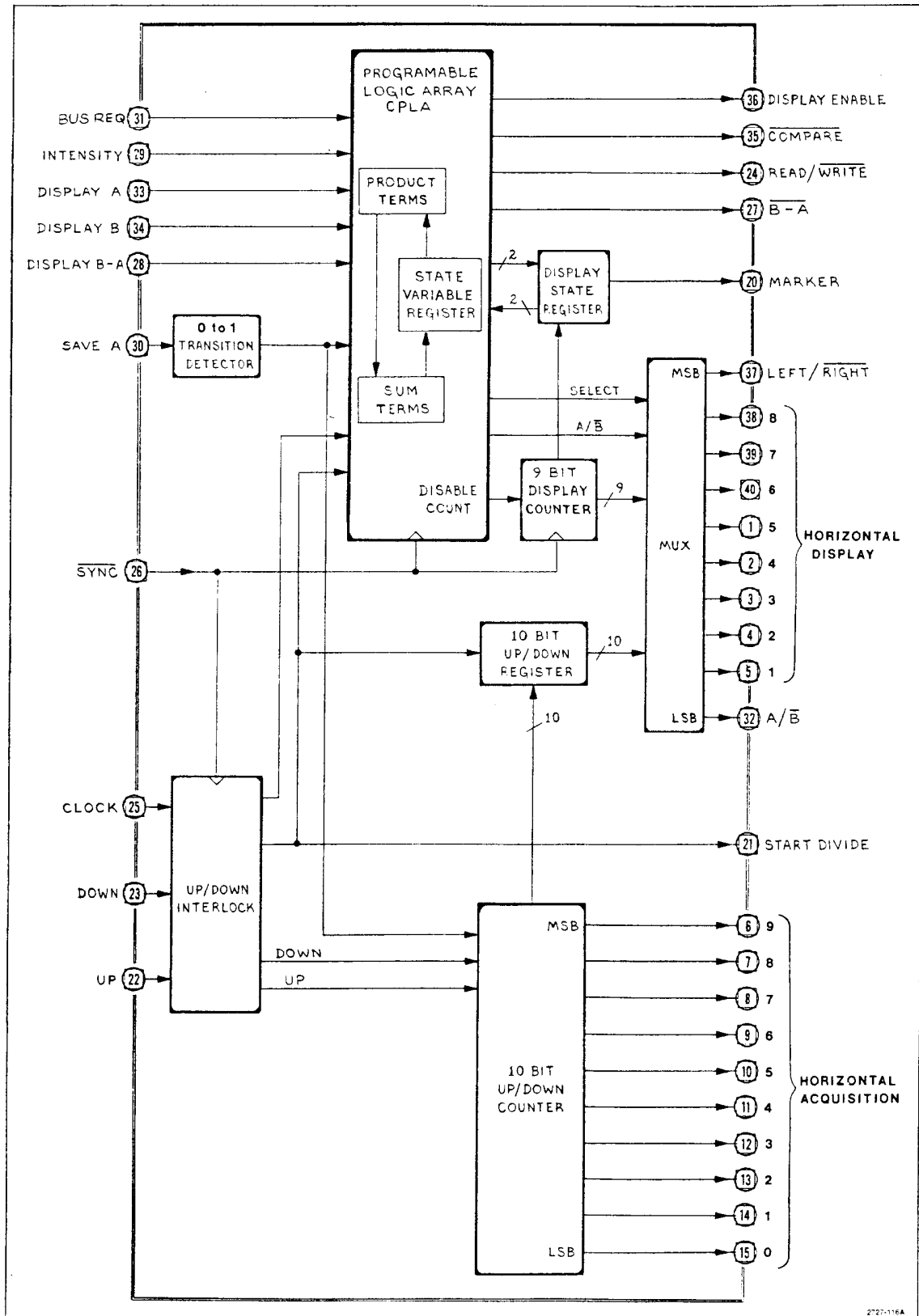
Fig. 5-16. Horizontal control IC block diagram.

fast retrace occurs. This retrace, unlike that following the A memory display (cursor), is not required to be seen and is thus blanked. This is accomplished by blanking control flip-flop U1014B, which is controlled by the most significant bit of the memory address and the display enable signal during a marker cycle.

Memories. Integrated circuits U1026 and U2026 provide 8k bits of random access memory for storage of the 1024 data points used in the digital storage system. Addressing is controlled by address tristate buffers U1022 and U1016 during display of memory data and by horizontal control IC U2032 during memory update.

DEFLECTION AMPLIFIERS ⟨26⟩

Refer to the block diagram adjacent to Diagram 26. The Deflection Amplifier selects from among several inputs to generate the drive signals for the crt plates, and generate a signal to drive the auto-focus portion of the Z-Axis circuit. Input signals are from the Horizontal Sweep, Readout, Video Filter, and Digital Storage circuits.

Horizontal Section

Signal lines HORIZ SIG (from the Digital Storage circuits) and SWEEP (from the Sweep circuit), through edge connector pins 49 and 51, are applied to switch IC U7055. One half of U7055, under control of the STORAGE OFF signal from the Digital Storage circuits, selects either HORIZ SIG or SWEEP inputs. When the STORAGE OFF line is floating or pulled high, the SWEEP signal is selected; when the line is pulled low, the HORIZ SIG signal is selected. The selected signal is then divided down from 1 V/div to 0.5 V/div by resistive divider R7051 and R7081 and buffered by U7073. From buffer U7073, a sample of the signal is applied to a rear panel connector via edge connector pin 48. The signal is also applied to the other section of switch U7055 along with the HORIZ R/O signal from the Readout circuits. Selection between these two signals is controlled by the R/O OFF signal, also from the Readout circuits, through edge connector pin 3. When R/O OFF is floating or pulled high, the signal from buffer U7073 is transmitted through the switch; when the line is pulled low, the HORIZ R/O signal is selected.

From U7055, the signal is applied to a shaper network to compensate for non-linearity in the crt deflection characteristics. This network consists of resistors R3051, R3052, R4059, R4058, R4057, R4062, R4061, and R3059, plus diodes CR4052, CR4051, CR4058, and CR3058. Note that HORIZ POS voltage from the front panel via edge connector pin 47 through resistor R2053 is applied to the shaper circuit so the shape correction factor relates to the crt deflection.

The shaped signal is then applied through preamplifier U2060 to the Deflection Amplifier circuits. The feedback path around U2060 includes Horiz Gain adjustment R1055 to calibrate the amount of compensation required for deflection sensitivity.

The horizontal deflection amplifier consists of two similar circuits, one for each horizontal deflection plate. One circuit is an inverting amplifier, the other operates in-phase. Inputs to the inverting side are through the parallel combination of resistors R3049, R3048, and capacitor C4057 to Q4038A. High-frequency response compensation is provided by the series connection of resistor R3048 and variable capacitor C4057. High-frequency feedback is controlled by capacitor C3043.

Input to the non-inverting side is through resistor R5029 to the base of Q4025A. R3019 and R5035 set the dc level for the feedback loop to the base of Q4025B. Variable capacitor C5021 provides adjustment to set transient gain. Again, high frequency feedback is controlled by capacitor C2021.

Gain of each amplifier section is approximately 20. (Horizontal deflection sensitivity of the crt is approximately 21.3 V/div per side.) Each section is single-ended and incorporates at the input side, a gain-degenerated dual (for temperature compensation) PNP transistor connected as a differential amplifier. For example, Q4038B of the right deflection amplifier drives emitter follower Q4047.

Signals with a low rate of change drive the output transistor through R5037, P3033. As the rate of rise increases, the drop across R5037 increases and when it reaches 0.6 V, either Q4035 or Q4042 are biased on. These transistors provide the high current drive for the output transistors. When the signal rate of change is low, Q1043 drives the crt deflection plate and Q1049 provides bias current for the amplifier. As the rate of rise increases, C3039 couples signal to the base of Q1049. Q1049 provides the positive drive to the deflection plate, Q1043 the negative drive. Each output transistor can provide a 200 V excursion in about 1 μs.

The horizontal amplifiers operate with approximately 1 mA of bias current in the output stage, as set by the current through resistor R3031 and the resistors connected at the base and emitter of output transistor Q1049. The current through resistor R3031 also provides the operating current for the dual input stage (Q4038A and B). Emitter follower Q4047 operates at approximately 2.5 mA. The output stage is degenerated for fast steps by emitter resistors R1045 and R1034. For a 0 V input, the output operating level is set by current from the −15 V source through resistor R4033. Dc feedback resistor R3045 sets this output level at approximately 142 V.

The above description of the right-hand (inverting) section is applicable to the left-hand (non-inverting) section except for the circuit element designations.

Output signals from the second half of switch U7055 are also supplied to the auto focus amplifier (IC's U6093, U6102, and transistors Q7097, Q7103). Amplifiers U6093 and U6102 produce a negative absolute value signal that is three times higher in amplitude than the signal from switch U7055. This amplified signal is then used to produce a shaped current by transistors Q7097, Q7103, and resistors R7102, R7101, R7107, R7108, to apply to the Z-Axis Interface circuit through edge connector pin 45. This signal will sink from 0 to approximately 0.8 mA of current from an external node at a voltage of approximately 0 V.

Vertical Section

Signal lines VIDEO FILTER OUT (from the Video Processor circuits) and VERT SIG (from the Digital Storage circuits), through edge connector pins 53 and 52 respectively, are routed through switch IC U6055. One side of U6055, under control of the STORAGE OFF signal from the Digital Storage circuits, selects either VIDEO FILTER OUT or VERT SIG. Note that the VIDEO FILTER OUT signal is buffered by IC U7065 to prevent changing load transients from affecting the signal level. When the STORAGE OFF line is floating or pulled high, the buffered VIDEO FILTER OUT signal is selected; when the line is low, the VERT SIG signal is selected. The selected signal is inverted and clamped to ground by U6065. (Both the VIDEO FILTER OUT and VERT SIG signals are specified at 0.5 V/div with 0 V for the baseline and positive voltages above the baseline. The signal is re-inverted and offset by buffer U6073 so center screen represents 0 V. From buffer U6073, a sample of this centered signal is applied to a rear panel connector via edge connector pin 46. The signal is also applied to the other side of switch U6055 along with the VERT R/O signal from the Readout circuits. Selection between these two signals is controlled by the R/O OFF signals; also from the Readout circuits. When R/O OFF is floating or pulled high the signal from buffer U6073 is transmitted through the switch. When the line is pulled low, the VERT R/O signal is selected.

The vertical section shaper (resistors R3061, R4065, R4067, R3071, R3064, and diodes CR4063, CR4064) and preamplifier (U2062) operate the same as the horizontal section. Transistor Q4078 limits positive excursions to approximately one division below the top of the screen to protect the output stages from being overdriven.

The vertical output stages are similar to the horizontal stages with the exception of higher bias current. Current flow of approximately 1 mA through resistors R3095 and R3098 result in approximately 5 mA in the output stages. Resistors R5081 and R5099 are of less resistance than

R5041 and R5027 in the horizontal section to correct for the increased current in dual input stage transistors Q4083 and Q4101.

Comparator U6024 compares the level of the signal from baseline clamp U6065 with a reference level set by divider R7032 and R7034 to produce the CLIP signal for the Z-Axis Interface circuits. The CLIP line is pulled low when the Video signal is more negative than the reference level (approximately 1 division above baseline), and pulled high by R7021 if the signal is more positive than the reference level.

Z AXIS CIRCUITS ⟨27⟩

Refer to the block diagram adjacent to Diagram 27. The Z-Axis circuits take the various beam control inputs such as SWP GATE, INTEN, etc., combine them, and furnish the drive currents and bias voltages required to operate the crt electrodes. The Z-Axis circuit consists of the Intensity Control Logic circuits, which control the crt beam current for normal signal display operations. It also includes the unblanking gates which furnish current to the Z-Axis Drive Amplifier to drive the crt control grid. The Z-Axis circuits also include voltage-setting circuits for astigmatism, crt trace rotation coil, geometry, and other crt electrode voltages.

Z-Axis Driver Amplifier

The Z-Axis Drive Amplifier Q3047, Q4058, and Q4059, is driven by two sources, exclusive to each other: U2038B/Q2042 drives the amplifier during readout display periods, and U2038A/Q2044 drives the amplifier during sweep display periods. U2039 is an AND-NOR gate that is connected to provide the logic to one input of NAND gate U2038A which turns Q2044 on or off. The R/O OFF line and the output of U2039 must both be high for U2038A to furnish current to Q2044. Table 5-8 lists the conditions under which U2039 will output a high to U2038A.

Table 5-8
U2039 TRUTH TABLE

U3046 output (line 28)	0	0	0	1	1	1	0	0	0
CLIP	0	0	0	0	0	0	1	1	1
Z Axis Blank	1	1	1	1	1	1	1	1	1
Storage Off	0	0	1	0	0	1	0	0	1
SWP GATE	1	0	1	1	0	1	1	0	1
U2034, pin 13	0	0	0	0	0	0	0	0	0

Only the combinations shown in the truth table plus a high on R/O line will gate a low out of U2038A. When

U2038A output is low, emitter current is furnished to Q2044, which in turn will furnish current through R2051 (the input resistance of the Z-Axis Driver Amplifier) to Q3047. U2034 is a single-shot that produces a 3 μs pulse to blank the crt beam during trace return between readout and signal display.

The other source of input current to the Z-Axis Drive Amplifier is Q2042. This transistor is turned on by U2038B when R/O UNBLANK is high and the R/O OFF is low.

Q1028 serves as a current source for the divider (R1030-R1025) that sets the operating point for Q2042 and Q2044 which sets the intensity level. Diodes CR1045 and CR1043, connected from base to base of Q2042 and Q2044, limit the display intensity by preventing the bases from going more positive than about 0.6 V above the emitter voltage of Q2022. This circuit, which includes the adjustment (R1027), sets the maximum current for both Q2042 and Q2044.

The Z-Axis Drive Amplifier is an operational amplifier consisting of transistors Q3047, Q4058, Q4059, and related components. The input resistance for the amplifier is R2051, and the feedback resistor is R3052. The output is clamped by diodes CR3059 and CR3066, to protect the amplifier from transient surges in case of crt arcing.

Transistors Q1017 and Q1015 provide current for the trace rotation coil. The adjustment (R1021) sets the current so the displayed trace is aligned with the graticule.

Transistors Q3045, Q4063, Q4065, and related circuitry are for use in future applications.

HIGH VOLTAGE SUPPLY ◇28◇

Refer to the block diagram adjacent to Diagram 28. The High-Voltage Supply furnishes the −3860 V to the crt cathode, the filament voltage for the crt, and provides dc restoration for the Z-AXIS DRIVE signal. The circuit consists of the following:

1) the high-voltage oscillator, which produces the crt filament voltage and the 200 Vac that is stepped up and applied to the voltage doubler circuit;

2) the voltage doubler, which rectifies and filters the high voltage for application to the crt cathode;

3) the high-voltage regulator, which samples the high voltage and regulates the operation of the high-voltage oscillator;

4) the Z-Axis clipper and rectifier circuits, which couple the Z-AXIS DRIVE signal to the crt control grid.

High Voltage Oscillator. This circuit consists of transistor Q1073, transformer T2065, and associated components. The output of the oscillator, approximately 200 Vac, is coupled across T2065, where it is stepped up for application to the Voltage Doubler, and stepped down for application to the crt filament.

Voltage Doubler. The voltage doubler consists of CR4041, CR4035, C4027, C5021, C4024, R3038, and R1039. The output of the doubler is taken off the anode of CR4035 and applied to the crt cathode. Reference voltage for the regulator is taken off the end of R1039.

High-Voltage Regulator. This circuit consists of amplifier U4083 and surrounding components. The high voltage is applied through a voltage divider consisting of R1017B and R1017C, which is connected through R1042 to +15 V. The sample of the high voltage at pin "U" is applied through R4075 to the input of comparator U4083. The correction signal, in the form of dc drive, is applied to the base circuit of Q1073 to set the oscillator current.

CR4078 and CR4077 at the input to U4083, protect the input against excessive voltage excursions. The circuit consisting of CR4071, R3079, and R4074 protect the oscillator if the +100 V supply should fail. Normally, CR4071 is back-biased. If the +100 V is not present, CR4071 conducts and clamps the input negative; the output of U4083 swings negative and Q1073 remains cut off. This circuit ensures that Q1073 will begin oscillating only after U4083 switches. CR3077 (in the output circuit of the regulator) prevents the base circuit of Q1073 from going negative.

Z-Axis Clipper. This circuit consists of diodes CR1056 and CR1046, plus associated components. 225 Vac from pin 8 of T2065 is coupled through C1058 and R1048 to the junction of CR1046 and CR1056. The regulator circuit consisting of VR1041 and R1051, hold the cathode of CR1046 at +110 Vdc. Thus, if the Z-AXIS DRIVE signal is +110 Vdc, the two diodes clip the incoming 225 Vac to a total excursion of 1.2 V. If the Z-Axis peak-to-peak voltage is at ground potential, the ac voltage at the junction of the two diodes swings from ground to +110 V. The voltage that passes the clipper circuit is coupled through C1031 to the Z Axis rectifier. The Z-AXIS DRIVE signal is also coupled directly to this circuit, where it is coupled through C1041 to the crt grid circuit.

The clipped Z-Axis drive signal is rectified by CR2044 and CR2046, which are the principle components of the second section of the Z-Axis circuit. The rectified voltage is then fed to the grid of the crt. C1041 couples the fast changes of drive voltage to the crt grid to speed up the response of the grid circuit. Neons DS2052, DS2054, and DS2057 protect the crt from high-voltage arcs from external

sources. R1044 and R1053 protect CR2046 and CR2044 respectively, from external high voltage surges.

CRT READOUT ⟨29⟩

The Crt Readout assembly stores readout characters and generates deflection and Z-Axis signals to display the characters. It also handles the frequency dot marker display. Both characters and frequency dot displays are time-shared with the spectrum trace.

Generating Readout

Crt readout is handled by sequential logic, clocked at 3.41 MHz, supplied by the Processor board. The readout circuitry (Fig. 5-17) comprises:

1) readout on timing, RAM for character storage;

2) character counter to access the RAM and control the scan;

3) character generator to unblank the crt beam;

4) D/A converters to deflect the crt beam;

5) instrument bus interface to store characters and control display. A more detailed block drawing is provided with the schematic, Diagram 29.

Up to 32 characters can be displayed in a line across the top of the crt and another line across the bottom; either of two sets of characters (page 1 or page 2) can be selected for display. Page 1 is used for normal front-panel readout; page 2 can be used for message input over the GPIB.

Readout-On Timing. Characters are drawn one at a time, allowing a portion of the spectrum to be drawn between each character. The character duty cycle is in the range of 10% to 25% because it varies with the character drawn. The time-sharing is pseudo-random, reducing the effect of gaps in the spectrum display by moving them on the trace.
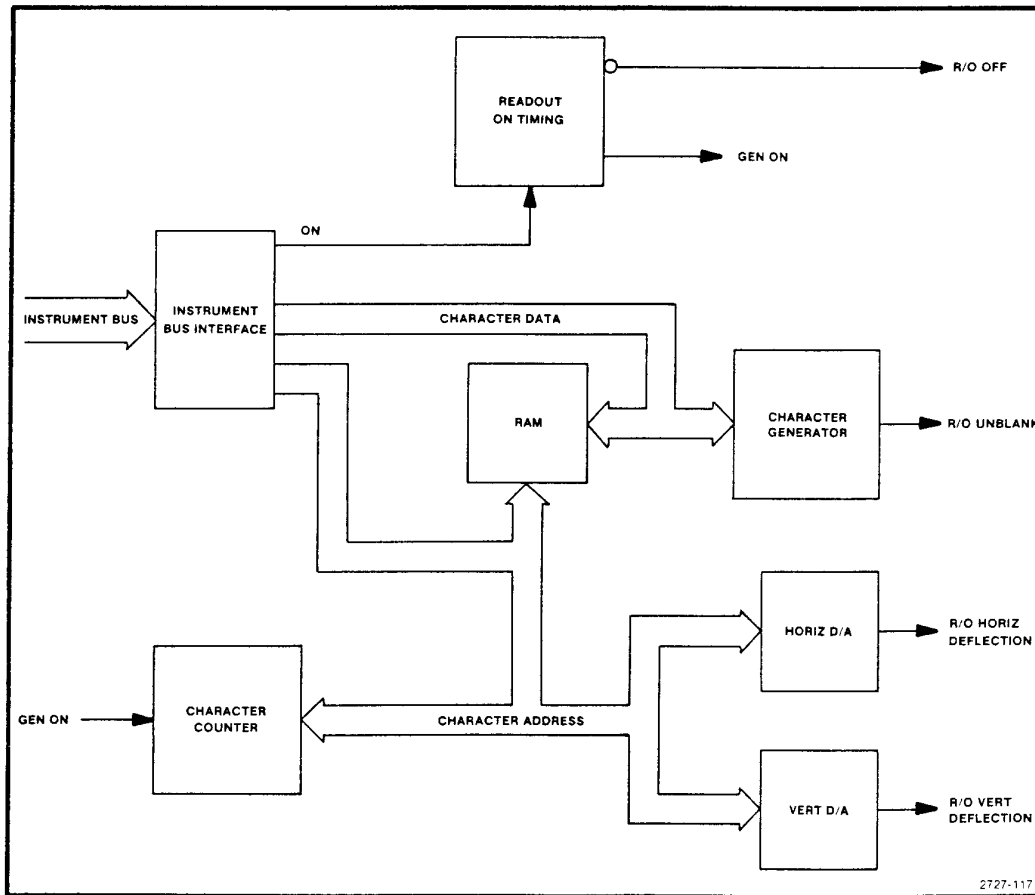

Fig. 5-17. Simplified crt readout block diagram.

The readout-off time is set to 175 μs by one-shot U2044 (Fig. 5-18). Flip-flop U2036B asserts GEN ON after U2044 times out, allowing a character to be drawn. When the character is finished, ROW 0, COL 0 resets the flip-flop, which retriggers the off-timer. The ON control bit must have been set by the microcomputer to get readout (as discussed below under Instrument Bus Interface).

If BLANK (MSB of the character data) is not set, the GEN ON flip-flop unasserts R/O OFF through AND-gate U1038B; this switches the readout deflection signals onto the deflection amplifier inputs on Diagram 26. BLANK can be set by the microcomputer as it loads a space into the character RAM so the readout does not use time for the spectrum trace to scan a blank character.

Character Scan. Although the 8678 character generator IC is often used in raster scans, in this application it is used to write complete characters, as shown in Fig. 5-19. A character is drawn as a pattern of dots in an 8 x 8 matrix where the top row and first three columns are blank. These blank dots allow for beam retrace and spacing. The idle position between characters is indicated on the figure.

Character counters synchronize the horizontal and vertical scan with the Z-axis signal from the character generator IC to draw the character. These counters, U2016, U2012, and U2018, are wired as a module 4096 counter to count the column (bits 0—2), the row (bits 3—5), and position of the character (bits 6—11). Bits 6 through 10 represent the horizontal position and bit 11 the vertical position (top or bottom). The position bits also address the character in RAM (assuming the readout is turned on by the microcomputer). The counters are enabled only when the generator has control of the crt beam (GEN ON) and INC is high; INC low stops the beam to write a dot on the crt.

The counters are wired to force the D/A converters to step through the character horizontally a row at a time. At the same time, the pattern of dots is accessed under the control of the timing decoder logic, U1022A and U1014. The AND-gate and decoder combine to control the character
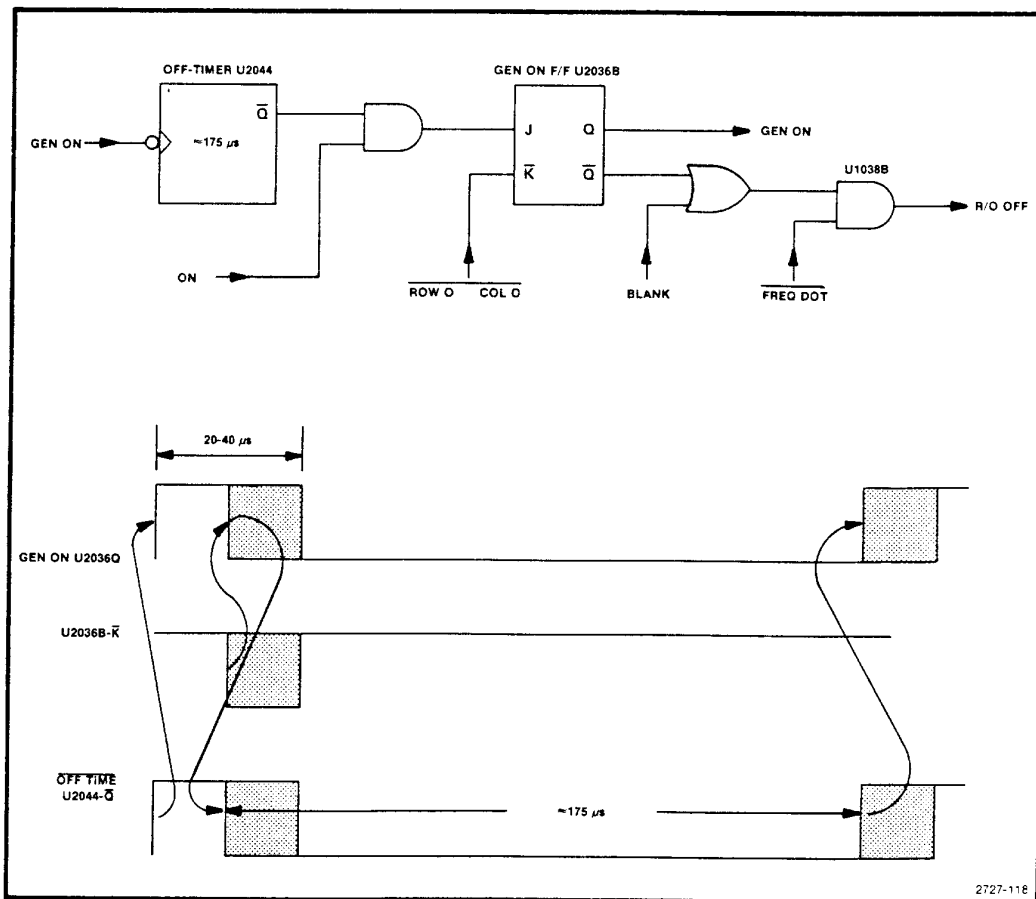
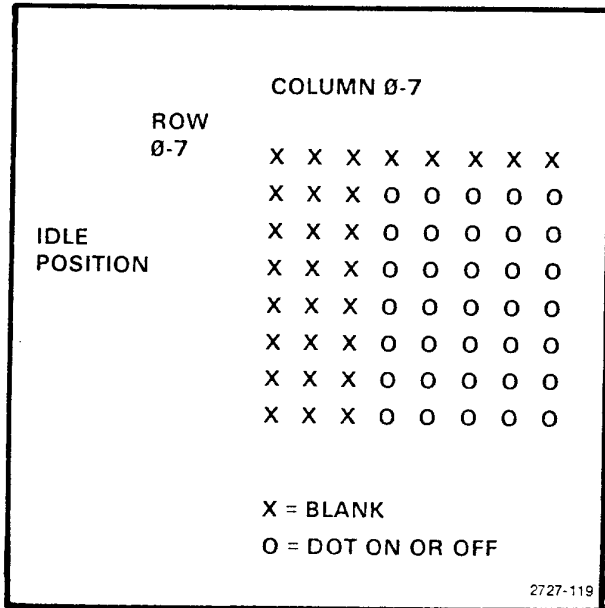

Fig. 5-18. Character on/off timing.

		COLUMN 0-7							
ROW 0-7		X	X	X	X	X	X	X	X
		X	X	X	O	O	O	O	O
IDLE		X	X	X	O	O	O	O	O
POSITION		X	X	X	O	O	O	O	O
		X	X	X	O	O	O	O	O
		X	X	X	O	O	O	O	O
		X	X	X	O	O	O	O	O
		X	X	X	O	O	O	O	O

X = BLANK

O = DOT ON OR OFF

2727-119

Fig. 5-19. Character scan.

generator (U1028), which generates the correct pattern of blanking to draw the pattern of dots for the character.

The 8678 (U1028) character generator IC (Fig. 5-20) contains a ROM with the correct pattern of 64 bits for each of the 64 characters in its repertoire. The bit patterns are accessed by a decoder that operates on the ASCII code on the character generator inputs. The pattern of bits is multiplexed one 8-bit line at a time into a shift register that is clocked out one bit at a time to control the crt Z-axis.

Character Generator Timing. The character generator timing lines are called DOT, LINE, $\overline{LE}$, and $\overline{CLR}$. Each cycle of DOT clocks one dot (bit) out of the shift register. A positive transition on LINE switches the next line (row) of dots onto the shift register inputs; the dots are latched by a negative transition on $\overline{LE}$ (load enable), setting up the shift register to display another row of dots. $\overline{CLR}$ resets the line counter to begin drawing another character.

DOT is ANDed from GEN ON, INC, and CRT CLK by U1022B. Inversion by the gate restores the phase relationship of the DOT input and the inverted clock used by the rest of the character generator. $\overline{LE}$ is gated by U1022A when the character counter reaches column 2. This loads the shift register with the next row of dots, which is displayed starting at column 3. LINE advances the line (row) counter after the scan of the current row begins to set up the next row of dots on the shift register inputs; this occurs at column count 4. $\overline{CLR}$ is asserted only once during the scan of each character. It is decoded by U1014 when the

character counter reaches row 1, column 0, the first non-blank row of dots scanned in each character.

See the character timing figure (Fig. 5-21) for the sequence of events to scan a character. At 1 on the figure, the character generator finishes a character. When the counter advances, decoder U1014 asserts $\overline{ROW\ 0}$ $\overline{COL\ 0}$, resetting the GEN ON flip-flop on the next clock. This stops the counter at row 0, column 1 (2 on the figure). When U2044 completes the time-out period and again sets the GEN ON flip-flop, the character counter resumes the scan, first causing $\overline{LE}$ (at 3) and LINE (at 4). Just before the scan enters the actual character area (at 6), $\overline{CLR}$ resets the character generator line counter (at 5). The break (7 on the figure) indicates that the scan continues. After the character is scanned, the scan returns to the idle state; 8 and 9 correspond to 1 and 2 on the timing figure.

Dot Delay. Each bit shifted out of the character generator is the value of a dot in the 8 x 8 matrix: 0 for a blank and 1 for a dot that is to be written. As the scan progresses at better than 3 MHz, a rather faint character display might be expected. To brighten the dots that are written, a shift register inserts some dot delay by stopping the counters while holding the crt beam unblanked. The dot delay timing is shown in Fig. 5-22.

A high on the character generator output (U1028-11) sets the dot delay shift register (U1036A,B,D) input high (assume Q of U1036C is high). It also sets the unblanking flip-flop (U2036A) J input high; once set, the flip-flop unblanks the beam during the rest of the dot delay cycle. Because the shift register must have completed any previous dot delay before entering a new cycle, the character generator high output also gates INC (increment) low at U1022C (assuming the microcomputer has turned on the readout). On the next clock, the highs on the two register inputs are latched.

Meanwhile, INC low puts the character counters on hold and disables the gate (U1022B) that clocks the character generator U1036C, the INC flip-flop, stores the low on INC at the next clock, putting a low on the dot delay shift register input.

Successive clocks propagate the dot through the shift register; when it emerges after three clocks, it is inverted by U1018C to reset the unblanking flip-flop and gate INC high. This sets U1036C again on the next clock. INC remains high if the value of the next dot is 0 or is gated low to repeat the dot delay cycle if the next dot is 1.
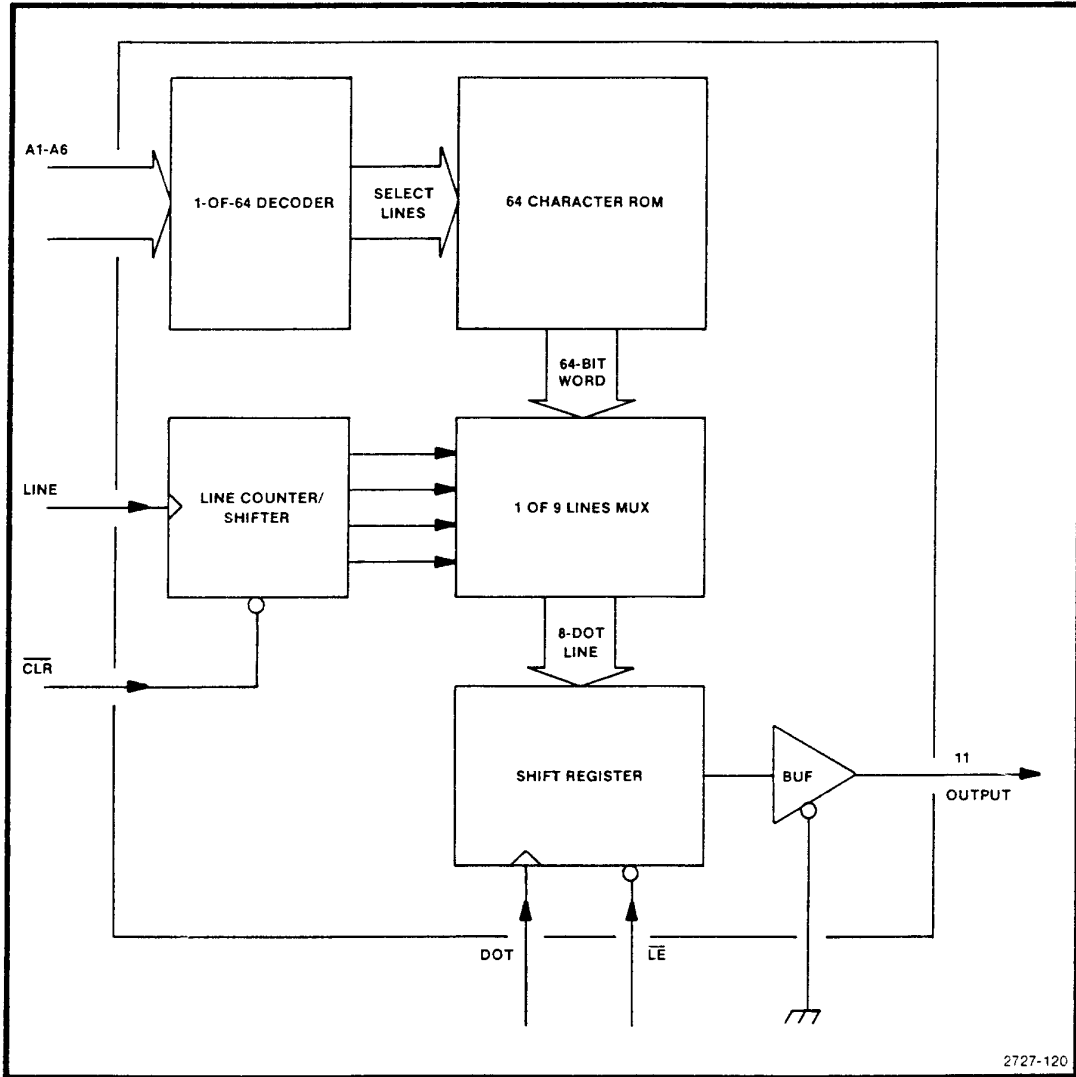
Fig. 5-20. Character generator (U1028) block diagram.

Instrument Bus Interface

The microcomputer controls the crt readout and frequency marker dot over the instrument bus through the following ports:

Port	Hex Address
Control	5F
Address/data	2F

Decoder U2038 asserts CONTROL when it sees a value of 5 on the upper four bits of the instrument bus address lines and $\overline{DATA}$ when it sees a value of 2. The decoder must be enabled by GEN ON low and DATA VALID high on the instrument bus. The false transition of DATA VALID causes the addressed port to latch the data on the instrument bus.

Control Port. The control port (U2034) turns the readout on or off, steers data sent to the address/data port, and controls the mode of the frequency marker dot. The lower four bits are defined (see Table 5-9). Bits are numbered in this discussion as on the instrument bus—starting at zero. However, the D and Q pins of U2034 (and some other ICs) are numbered as on their data sheets, starting at one.
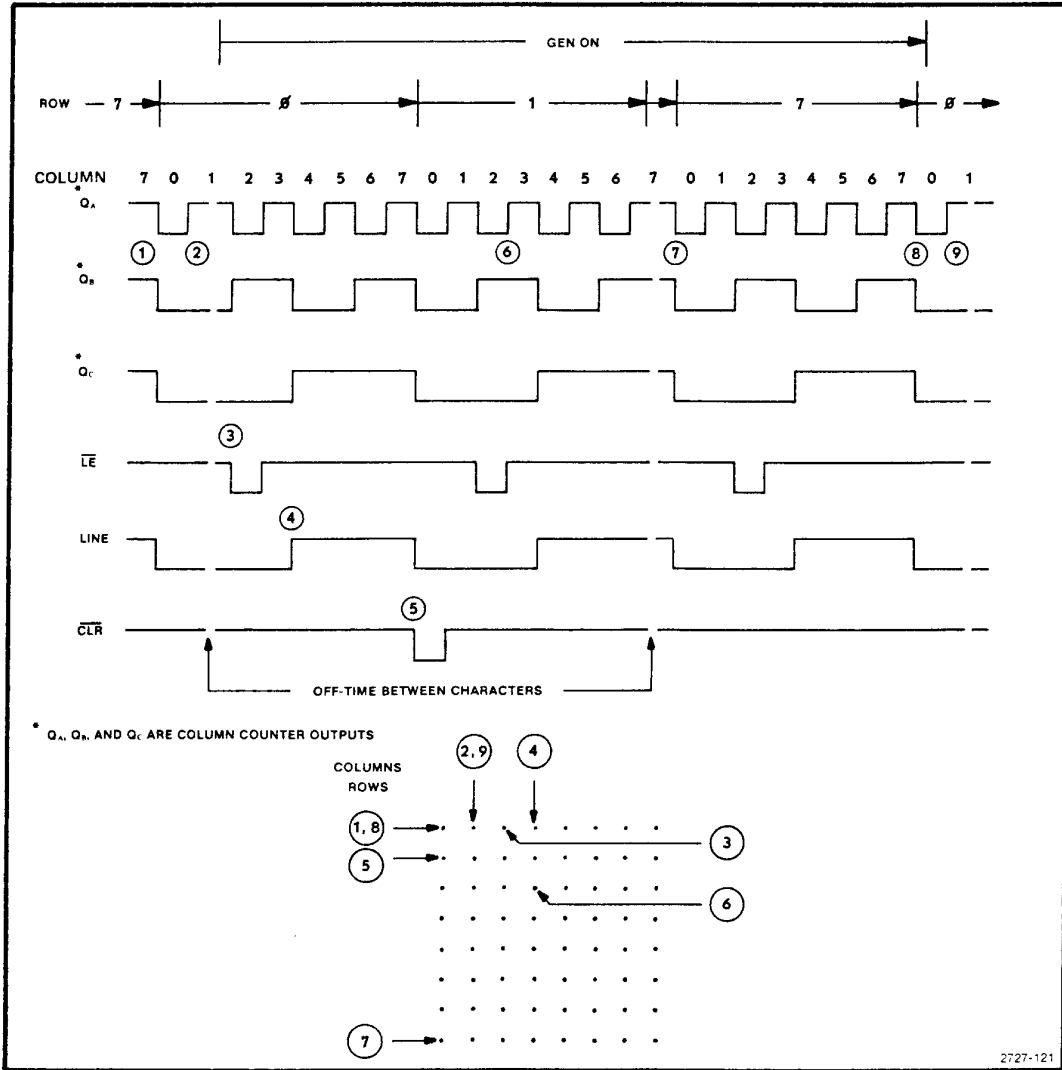
Fig. 5-21. Character scan timing.

Bit 0 turns the crt readout display on (1) or off (0). When set, this bit gates the off-timer to the GEN ON flip-flop J input through U1038D, enables the INC gate (U1022C), and steers the position counter onto the character RAM address inputs through multiplexer U1024. When cleared, this bit places an address, latched in U2024, on the character RAM address inputs.

Bit 1 interprets data sent to the address/data port as an address (1) or data (0) for the character RAM. Setting this bit disables the character RAM for input and sets up the clock signal to latch the address.

When this bit is set, $\overline{Q2}$ of U2034 gates a high on the output of U2032A. This high prevents input to the character

RAM (U1026) by setting its R/$\overline{W}$ input high. This high also disconnects the instrument bus from the character RAM data inputs by disabling U2028. Meanwhile, $\overline{Q2}$ of U2034 is low, enabling U2032D to gate the clock signal that latches the address. The positive clock transition is applied to U2024 when DATA VALID goes false at the end of a write cycle to the address/data port, releasing $\overline{DATA}$.

When this bit is cleared and $\overline{DATA}$ is asserted, U2032A enables the character RAM for input and passes the data through U2028.

Bit 2 selects information from the two halves of character RAM space. When set, this bit selects page 1, the normal front-panel readout. When cleared, this bit selects page 2, a
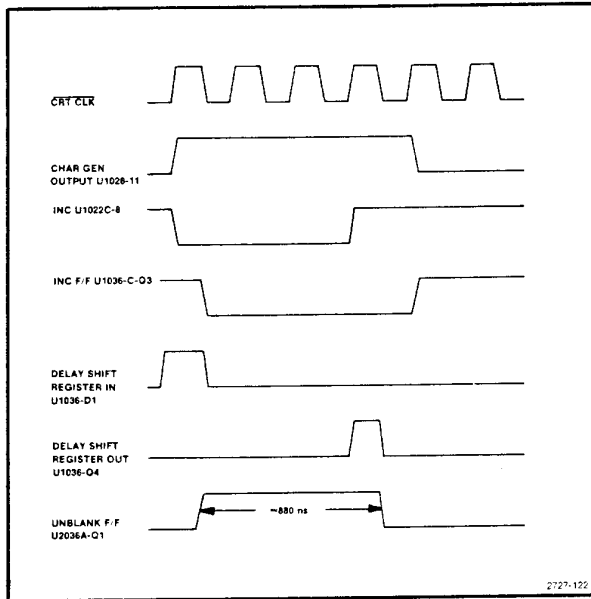
Fig. 5-22. Dot delay circuit timing.

64-character space that may be loaded with messages via the GPIB.

Table 5-9
CONTROL PORT

Bit	Function
0	Readout on/off
1	Address/data
2	Page 1/page 2
3	Max Span dot

Bit 3 controls the frequency dot marker. This bit is set in MAX SPAN mode to position the frequency dot with BFRD TUNE VOLTS from the first local oscillator. When cleared, this bit centers the frequency dot on the spectrum display.

Address/Data Port. The microcomputer loads characters for crt display through the address/data port. Each character requires four write cycles:

1) bit 2 in the control port is set for an address transfer;

2) the address in character RAM is sent to the address/data port;

3) bit 2 in the control port is cleared; and

4) the data is sent to the address/data port. The bits are defined in Table 5-10. Bits 0—5 are the lower six bits of the character RAM address or are the ASCII code for the character.

Table 5-10
ADDRESS/DATA PORT

Bit	Function
0—5	Address of ASCII code
6	Vertical shift
7	Blank

Bit 6, when set, shifts upper readout characters to the center of the crt (and lower readout characters off the bottom of the screen). This may be used with page 2 characters to give prominence to a message sent to the operator.

Bit 7 is used to reduce readout display overhead. It is set when a space is transferred to the character RAM so the readout does not steal time from the spectrum trace to scan a blank. When set, this bit prevents the GEN ON flip-flop from gating R/O OFF low through U2032C.

Frequency Dot Marker

The frequency dot marker is refreshed immediately after the last character position in the lower readout is scanned. Normally, the marker is centered on the screen just below the upper readout as a pointer for the center frequency readout. When MAX SPAN is selected, however, the dot marker moves to a point on the display that corresponds to the center frequency value.

The negative transition of TOP triggers the marker generator. A simplified diagram of the circuit and its timing is shown in Fig. 5-23.

U2042A delays the marker dot to allow retrace while gating FREQ DOT low to set up the display. FREQ DOT affects the readout deflection outputs in the following ways.

The horizontal output is connected either to ground for a center-screen dot or BFRD TUNE VOLTS for a max span pointer. TUNE VOLTS is proportional to the center-frequency readout offset from the center of the frequency range.

Bits 4 and 5 at the vertical D/A input are asserted to shift the crt beam below the upper readout (the row counter inputs are zeros).

R/O OFF is gated low to switch the deflection amplifier inputs for a display using the marker dot horizontal and vertical signals.
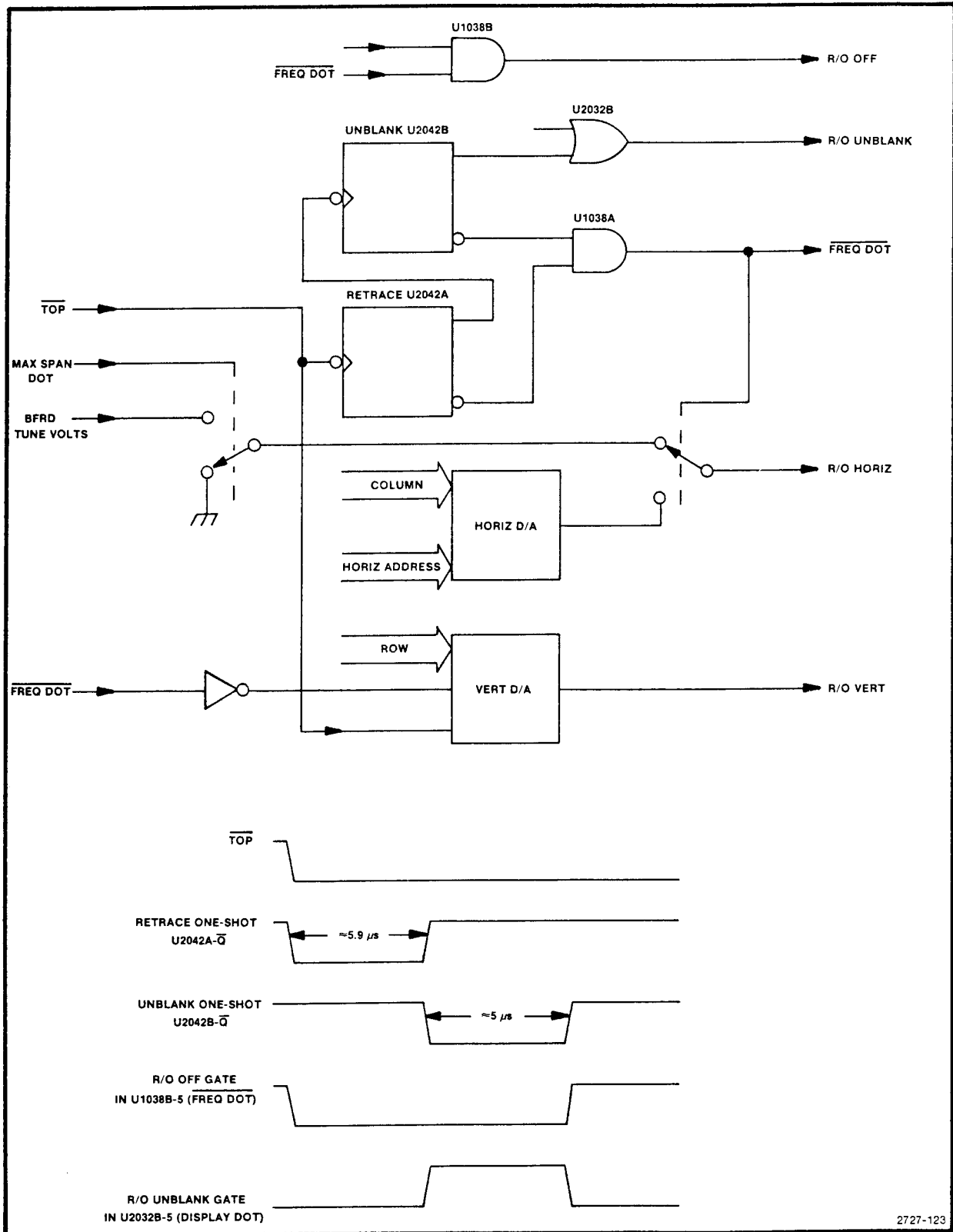
Fig. 5-23. Frequency dot marker circuit and timing.

2727-123

When the retrace one-shot times out (about 5.9 μs), it triggers the unblanking one-shot, U2042B, which sets R/O UNBLANK high for about 5 μs. This refreshes the dot. The corresponding low on the one-shot's inverted output holds FREQ DOT low until the dot marker is drawn. CR1041, R1041, and C1041 slow the rise on the other input of U1038A to prevent a spurious signal on FREQ DOT.

⟨7⟩
FREQUENCY CONTROL SECTION

The Frequency Control section performs the tuning and sweeping (scan) function for the Preselector, 1st LO (Local Oscillator), and 2nd LO. It contains the following major circuits.

Sweep. The Sweep circuit accepts trigger inputs from line, internal, and extenal sources in addition to the normal free-run mode of operation. It also receives external horizontal and manual sweep inputs. The circuit produces a PEN LIFT signal for chart recorder applications, a SWEEP GATE signal for crt display blanking, a SWEEP signal to drive the crt horizontal axis and digital storage circuit, plus a ramp for the Span Attenuator circuits and eventually the Preselector, 1st LO and 2nd LO.

Span Attenuator. This circuit inverts and attenuates the incoming ramp signal, as required to sweep the 1st and 2nd Local Oscillators, and the Preselector.

Center Frequency Control. The Center Frequency Control circuit provides a tuning voltage for the 1st and 2nd Local Oscillator circuits that results in a linear center frequency change as the front panel FREQUENCY control is changed. The circuit is directly controlled by the microcomputer, so remote control of the frequency is possible, by way of the GPIB rear-panel connector. The COARSE TUNE VOLTS signal from this circuit is applied to the 1st LO Driver circuits for summing with the SPAN signal to drive the 1st LO. The FINE TUNE VOLTS signal is applied to the Preselector Driver for summing with the IF Offset voltages, and to the Shaper and Bias circuits for summing with the 2nd LO SWEEP signal.

1st LO Driver. The 1st LO Driver performs the following:

1) combines the COARSE TUNE VOLTS signal with the SPAN signal and produces current to drive the 1st LO;

2) produces the tuning and sweeping signal for application to the Preselector Driver circuits;

3) produces the mixer bias voltages;

4) produces the BUFFERED TUNE VOLTS signal that is applied to the Display section;

5) produces a reference voltage that is used in both the 1st LO Driver circuit and the Preselector driver;

6) produces a supply voltage for the 1st LO.

Preselector Driver. The Preselector Driver is included as part of Option 01. The circuit combines the FINE TUNE VOLTS signal, the PRESELECTOR DRIVE signal, and the SPAN VOLTS signal. This combined signal is offset to compensate for the selected 1st IF then shared to drive the Preselector so it tracks with the 1st or 2nd LO. Also, the Preselector Driver drives a switch that selects either the Preselector or the Lowpass Filter, depending on the 492/492P operating frequency.

Shaper and Bias Circuits. The Shaper and Bias circuits, depicted on Diagram 38, are split between two systems. The Bias circuits are considered to be part of the 2nd Converter System, so they are described with that system.

The Shaper circuit combines the 2nd LO SWEEP and FINE TUNE VOLTS, then shapes the resultant to produce a non-linear drive signal for the 2nd LO. Because of oscillator characteristics, this non-linear voltage provides a linear frequency change with input voltage.

SWEEP ⟨33⟩

An overall block diagram of these circuits appears adjacent to Diagram 33. The Sweep circuit provides the ramp signal to drive the Horizontal Deflection Amplifier, the 1st Local Oscillator Driver, and the Preselector Driver (Option 01). The sweep generator also provides signals for an external plotter pen, the Z-axis, and digital storage circuits.

The Sweep circuit consists of four major circuits:

1) the digital control circuits, which receive and decode the address and instructions from the microcomputer, select the sweep rate, holdoff time, trigger source, sweep mode, and control interrupts to the microcomputer;

2) the trigger circuits, which process and multiplex the three trigger signals;

3) the sweep generator, which generates the voltage ramp that drives the Deflection Amplifiers, Digital Storage, and the swept oscillators;

4) the sweep control circuit, which generates the SWEEP GATE and PEN LIFT signals, and determines the holdoff time for the sweep generator.

Trigger Circuits

The sweep generator can be triggered from three sources: internal, external, and line signals. All three signals are converted to TTL levels by input buffer stages. Each output signal is coupled to U3034, the trigger multiplexer.

The external trigger signal (EXT TRIG/HORIZ IN) is capacitively coupled from the external trigger input connector through a compensating network to the input of the external trigger buffer and level shift circuit, which consists of differential amplifier Q2084 and buffer U1052E which converts the signal to TTL level. Diodes CR2075/CR2086 protect the input stage from excessive voltage.

The signal for the internal trigger circuit (VIDEO FILTER OUT) from the video filter is applied through Q2074 coupled to differential amplifier Q1078, then converted to TTL levels by U1052F. CR1088 and CR1089 protect the input of Q1078 from excessive voltage.

The input line trigger signal amplitude is large enough to overdrive Q1047 producing a line trigger output 0 to +5 V peak. Diode CR1035 protects the emitter-base junction from reverse bias.

Upon instructions from U2043, the "2" side of dual trigger multiplexer U3034 selects the trigger signal for the clock input of trigger flip-flop U2034B. The flip-flop clocks on the rising edge of the applied signal, so the complement of the signal at the D input appears at the output at the first trigger after the multiplexer enable goes to a low state.

Upon instructions from U2043, the "1" side of U3034 selects either the output of U2034B or the high state at pin 6. When the multiplexer is disabled, which occurs during sweep holdoff time, the multiplexer output is low. If free run is selected, the output goes high as soon as the multiplexer is enabled. However, if the sweep is in a triggered mode, the output will not go high until the next trigger occurs. This transition restarts the sweep. When the sweep starts again, U2034B is set by sweep state flip-flop U5026A in preparation for the next sweep end-holdoff-trigger cycle.

Sweep Generator

The sweep generator consists of the timing current generator (timing resistor selector U6102, voltage regulator U4095, U6092B, and surrounding circuitry), the integrator (U4101, U5085C, Q3100, U5085A, Q3090, U5085D, Q3095, and associated components), and the reset clamp (U5085B, Q2107, and surrounding circuitry).

The timing reference voltage for the sweep circuits is set by U4095 to −10 V. Divider R5092—R5094 sets the voltage at the non-inverting input of U4101 to −8 V; feedback sets the inverting input at the same potential. This input is driven by the output of multiplexer U6102. Operation of the circuit is as follows: The 1 to 10 V reference, from U4095, is applied to U6092B, which changes this level to −12 V, which connects to one side of the timing resistors connected to U6102. A 4 V difference then appears across the timing resistor. Multiplexer U6102 decodes instructions from U3042 (the 0F port latch), and connects only one resistor or resistor pair to its output pin, which then becomes the current source for integrator U4101. The multiplexer input codes for each of the sweep rates are listed with the description of the Digital Control circuits. Sweep accuracy adjustment R5105 is set to compensate for errors in this voltage or in the timing capacitor values. The timing capacitors are matched, so one adjustment can be used for the entire set.

The timing current furnished by the multiplexed resistors varies such that 1/l is proportional to a 2—5—10 sequence. Decade switching of sweep rates is provided by timing capacitor selection (C3079, C2094, and C2098). C2098 is used in all sweep rates, and for the 20 μs to 1 ms range. When a sweep rate of 2 ms to 100 ms is selected, the output of open collector comparator U5085D goes high, causing FET Q3095 to conduct and place timing capacitor C2094 in parallel with C2098. Likewise, when a sweep rate of 200 ms to 10 s is selected, U5085A causes Q3090 to switch C3079 in shunt with the other two capacitors. (The 10 s/div sweep rate is only used in the auto-sweep routine, or in the 492P.) VR2093, R2099, CR2101, CR2102, and CR2103 clamp the output to prevent the negative sweep retrace from causing the FETs to conduct.

A voltage divider consisting of R2012, R2013, and R2017 set a switching threshold of about +7.4 V at the input of the right-of-screen comparator U2015B. At the beginning of the sweep, the output of integrator U4101 is −8 V. The output voltge rises linearly to +7.4 V, then U2015B switches, placing a low at the input to U5016B. This causes the output PEN LIFT signal to move high. This signal was low up to this point, because of the high SWP GATE signal at the beginning of the sweep cycle and the high level at the output of U2015B. The PEN LIFT signal switches before retrace occurs to give the pen time to lift. The sweep rises in amplitude until it reaches +8 V, causing U2015A (the end-of-sweep comparator) to switch. (The same divider that was mentioned earlier sets a switching threshold of about +8 V at the non-inverting input of U2015A.) The low state from U2015A is inverted by U1052A and the high output applied to U4016A sets U5026A. The high state at the Q output of U5026A is inverted by U4016B, causing the SWP GATE signal to move low, blanking the crt display. The low out of U4016B also gates PEN LIFT high through U5016B.

The low state now at the $\bar{Q}$ output of U5026A is coupled to the holdoff circuits and the inverting input of U5085B, an open collector comparator. U5085B switches, its output rises, and Q2107 conducts. This clamps the output of the integrator to its input, and discharges the timing capacitors. Q2107 continues to conduct until a trigger is furnished to U4016C, which resets U5026A to begin the next sweep cycle.

When manual scan or external sweep is selected, both inputs to U5016D are high, which causes its output to be low. This causes the output of comparator driver U5085C to switch high and turn FET Q3100 on. As a result, feedback resistor R3105 is placed across U4101, converting it into an amplifier. Timing capacitor C2098 is still in the circuit, but its small capacitance has negligible effect at the low frequency of operation in this mode. The output of U5016C also resets U5026A and the SWP GATE remains high. These levels will remain until the output of U4101 overcomes the switching point of U2015A.

The input signals from manual scan and external horizontal are multiplexed by U6102 and applied to U4101. Since the summing node of the amplifier is not at ground, R7091 and R4093 shift the dc levels of the manual and external drive signals, respectively. U6092A is an inverting buffer for the external voltage; VR6086 is for overvoltage protection.

The sweep ramp from U4101 is applied through voltage divider R6058—R6052, which reduces the ramp voltage to U6061 to 11 V, centered around 0 V. The output of U6061 is applied to the Digital Storage and Deflection Amplifier circuits. The extra volt of sweep amplitude is used to deflect the beam 0.5 division off screen on each side.

The sweep signal from U4101 is also applied to U6071, which amplifies the ramp to 22 V, centered around 0 V. This signal drives the Span Attenuator and ultimately the 1st Local Oscillator.

Sweep Control

This description is based on the assumption that the sweep is in neither the manual nor the external mode. At the end of the sweep, U5026A is in set state. Its $\bar{Q}$ output is low, which causes the output of U4026C (the holdoff generator) to switch high. This starts the holdoff cycle. The holdoff time between sweeps must be sufficiently long for the timing capacitors to discharge and for any transient responses in the swept circuits to die. As the sweep time increases, the holdoff time is increased.

When the output of U4026C rises, the holdoff capacitors charge to +5 V through R3027. Capacitor C1013 is always

in the holdoff circuit. When U2043 latches Q4 or Q5 high, this produces a low out of U4026F or U4026E which increases holdoff time by adding C3028 or C3027 into the holdoff circuit. Diodes CR3034 and CR3035 protect the two inverters from reverse voltage transients that might pass through the capacitors.

When the voltage on the capacitors reaches +5 V, the output of U2015D switches high. If single sweep has not been selected, both inputs to U3061C will now be high and its output will enable trigger multiplexer U3034. When the next sweep is ready to run (depending on the trigger selection conditions), pin 7 output of U3034 switches high. This change in state gated through U4016C resets U5026A and begins the next sweep cycle.

When the single sweep mode has been selected, pin 2 of U5016A is high. U2034A, the single-sweep flip-flop, must furnish a low to U5016A to enable U3034 to trigger a single sweep. This enabling occurs when the microcomputer clocks U2034A. When the sweep starts, U5026A resets and sets U2034A. This ensures that only one sweep occurs for each microcomputer command.

Single-sweep mode is usually selected by front-panel commands; however, in some modes, the microcomputer will command single sweep. The microcomputer can also abort a sweep and start another with the next trigger; a pulse from U5052C, through U3061B, to pin 3 of U4016A sets U5026A and causes the sweep circuit to reset.

Digital Control Circuits

As mentioned throughout this description, the sweep is controlled by latched codes and pulses. The board has two ports for receiving information from the microcomputer, addresses F and 1F. U5033 buffers the data inputs, decreasing the loading instrument bus. Address decoder, U5043, decodes the address bus and strobes the data onto the board. Each output of U5043 goes to low when the corresponding port is addressed. Data is latched on the rising edge of this strobe, which is the trailing edge of Data Valid. The output of U5043 is inverted (U1052B inverts 1F; U1052C inverts 0F), then combines with the proper data bus line to form each bit of pulsed data. The pulse is at the low state for the duration of the Data Valid pulse (approximately 1 μs).

U3042 latches the data from port 0F. The combinations of D3 to D7 select the sweep rate; D3 and D4 control timing capacitor selection, and D5 to D7 control timing resistor selection. Table 5-11 lists the sweep rate selection codes. D2 is high during single sweep operations; otherwise, it is low. D0 commands a single sweep cycle.

Table 5-11
SWEEP RATE SELECTION CODES

Sweep Rate	D7	D6	D5	D4	D3
20 μs/div	1	1	0	1	1
50	1	0	1	1	1
100	1	0	0	1	1
200	0	1	0	1	1
500	0	0	1	1	1
1 ms/div	0	0	0	1	1
2	1	1	0	0	1
5	1	0	1	0	1
10	1	0	0	0	1
20	0	1	0	0	1
50	0	0	1	0	1
100	0	0	0	0	1
200	1	1	0	0	0
500	1	0	1	0	0
1 s/div	1	0	0	0	0
2	0	1	0	0	0
5	0	0	1	0	0
10	0	0	0	0	0
Manual	1	1	1	1	1
External	0	1	1	1	1

U2043 latches the data from port 1F. Line Q6, when high, enables an interrupt to the microcomputer at the end of a sweep. This is done as follows: At rest, U2024A is reset and the low at its Q output holds U2024B in the set state. When the sweep ends (which constitutes an interrupt event), the positive edge out of inverter U1052A clocks U2024A to the set condition and the $\overline{Q}$ output of U2024A, through inverter U3061A causes Q4052 to conduct, forcing $\overline{SER\ REQ}$ low. The microcomputer responds by setting the interrupt read line low; that is, it polls all addresses serially, which eventually places a high at AB7 and POLL simultaneously (Fig. 5-24). This causes a high at the output of U4016D (the $\overline{Q}$ of U2024A is low, since the flip-flop is now set), and saturates Q4051, pulling the D4 line low (this identifies the sweep board as the service request originator). Now, the microcomputer clocks an interrupt clear pulse to reset U2024B. This in turn, resets U2024B which sets U2024A. The circuit has returned to its reset stage.

U5052A and U5052B produce the interrupt read and clear signals. When the microcomputer wants to read or clear, it sets the POLL line high. Address bus line AB7 is high to read, resulting in a low at the output of U5052A. AB7 is low to clear, which results in a high at the output of U5052B.

SPAN ATTENUATOR ⟨35⟩

The Span Attenuator, under control of the microcomputer, selects the appropriate attenuation factor for the incoming sweep signal, to establish the frequency span. Refer to the block diagram adjacent to Diagram 35. The Span Attenuator consists of digital control circuits, which receive and decode the address and instructions from the microcomputer; the input amplifiers, which perform noise reduction and signal inversion on the incoming sweep signal; the digital-to-analog converter, which attenuates the sweep signal to the desired amplitude for driving the 1st LO Driver and Preselector Driver circuits; and the decade attenuator, which provides three decades of attenuation for the output signals.

Digital Control

Decoder U5025 decodes the address information from the address bus and sends a low signal to either of the two latches, U1025 (address 75) or U2015 (address 76), when a latch is addressed and the DATA VALID line moves high. (The data is stored in the latches on the trailing edge of the DATA VALID signal.) Logic buffer U4015 reduces loading of the data bus. Latch U1025 stores data that controls the eight least significant digits of the span attenuation factor. Latch U2015 stores data that controls the two most significant digits of the span attenuation factor, and other functions on the board. When a span attenuation factor is selected, the microcomputer selects an address and places the first byte of the data on the bus. The DATA VALID signal causes the data to be stored in one of the two latches. Then the second address is called and the next byte is stored in the other latch. The block diagram illustrates the significance of each bit in tables near the affected circuit. A logic 1 represents the more positive of two levels or high state, and a logic 0 represents the more negative of two levels or low state.

Input Section

The sweep signal and its ground reference are applied to differential input buffer U3036. Any signals or noise induced in the two signal transmission paths are cancelled by this stage.

The following stage consists of amplifier U3032, plus switching transistors Q2025, Q2028, and Q2023. Different mixing modes require the 2nd LO frequency to either in-
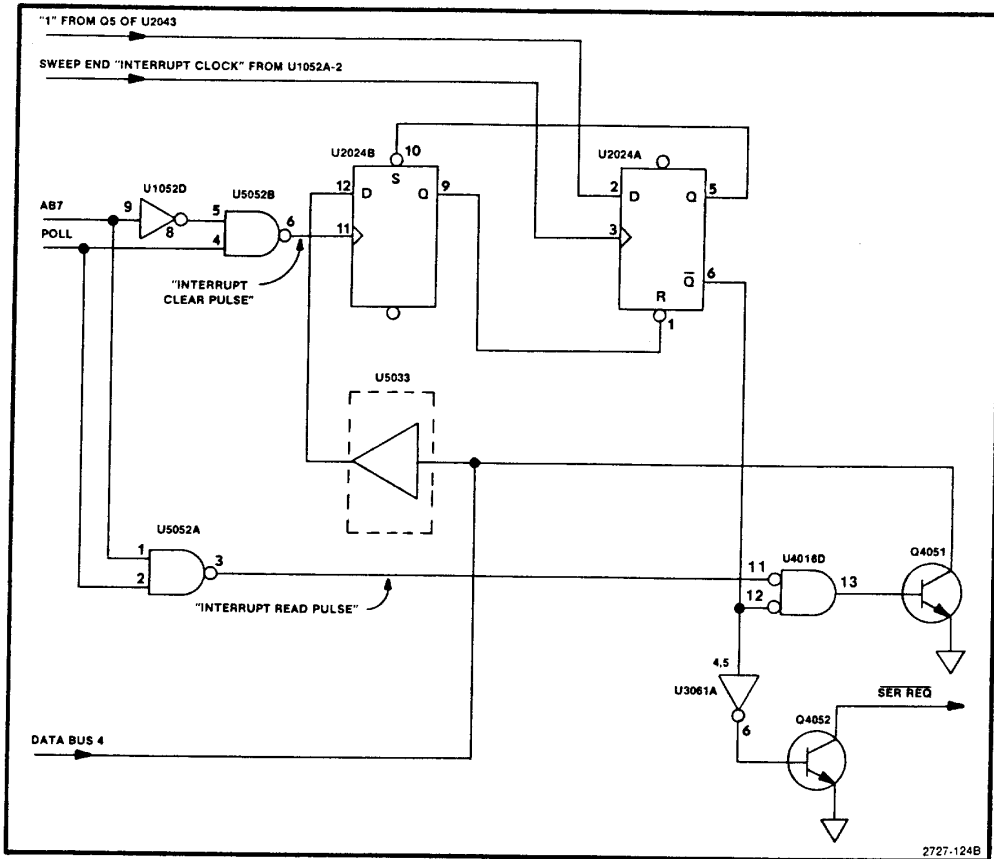
Fig. 5-24. Sweep "interrupt" circuits.

crease or decrease to increase the signal frequency. Thus, this circuit is a unity gain amplifier that can be changed from inverting to non-inverting under bus control. When line Q8 of latch U2015 is low, Q2023 conducts more and its collector moves positive to about +5 V. This in turn causes both Q2025 and Q2028 to conduct. Pin 3 of U3032 is effectively grounded, the sweep signal is applied through R3022 to the summing node of the amplifier, and the gain of the stage is −1. If line Q8 is high, Q2023 does not conduct and the voltage at its collector falls to nearly −15 V. Neither Q2025 nor Q2028 are now in conduction, so the sweep signal is applied to pin 3 of U3032, and pin 2 is disconnected. Now, the gain of the stage is +1.

Digital-To-Analog Converter

The magnitude of the sweep signal is determined by the desired frequency span, band, and option installed in the instrument. The microcomputer calculates the proper magnitude for each combination, and sends the appropriate codes to the data latches, which in turn control the attenuation factor of the digital-to-analog converter. This stage consists of converter U1042, amplifier U2042, and a complementary pair, Q2062 and Q3056, that form the output current buffer.

Figure 5-25 illustrates a simplified two-bit digital-to-analog converter. The circuit works by current division. Since the summing node of the amplifier is at ground potential, the magnitude of the current through a resistor is not affected by the position of the switch that selects that resistor. For example, when switch S1 is at position B, the current is shunted to ground. When S1 is at position A, the current through R1 becomes part of the total output current. Thus, the output current can be 0, 1/4, 1/2, or 3/4 of the total current available. Because of the resistance ratios, the ratio of the output voltage to the input voltage equals the ratio of the output to the total current ($V_{out}/V_{in} = I_{out}/I_{total}$). In this 2-bit converter, there are 2^2 or 4 output values possible. In the actual 10-bit converter, there are 2^{10} or 1024 output values ranging from 0 to 1023/1024 of the input.

In converter U1042, each internal resistance is switched in or out by a CMOS FET (internal to the device). The
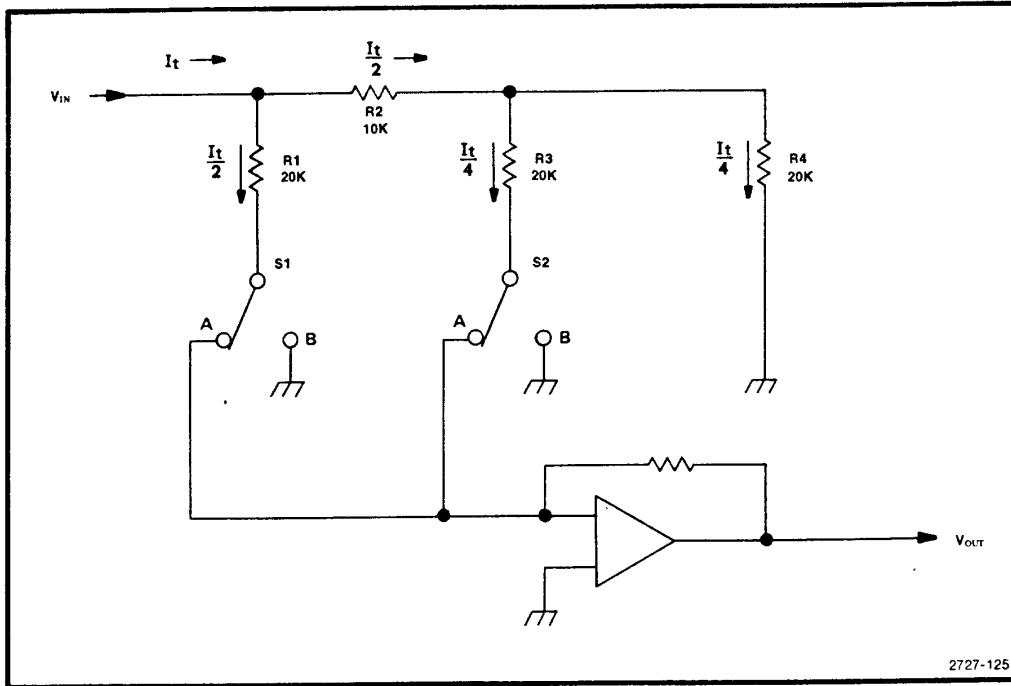
Fig. 5-25. Simplified digital-to-analog converter.

CMOS inputs are each protected by a series input resistor. Since the sweep signal is applied to the V_{ref} input, U1042 serves as a digitally controlled attenuator for the sweep signal.

The attenuated sweep signal from U1042 is applied to U2042, an operational amplifier. It in turn drives an output current buffer, consisting of complementary pair Q2062/Q3056. The pair is biased to produce an output current of about 10 mA in the absence of an applied signal. This eliminates crossover distortion of the output signal. Diodes CR2051, CR2053, CR1051, and CR1049 provide temperature stabilization for the bias current in the stage. When high current is passing through the pair, diodes CR1056 and CR1061 clamp the voltage across the emitter resistors to reduce voltage drop.

Feedback for the output stage is provided by R1056, plus an internal resistor in U1042. The internal feedback resistor ensures better temperature tracking. The internal resistor provides a gain slightly less than unity; R1056 increases the stage gain and permits gain calibration, as described below.

One-of-four decoder, U4025, using the data from the Q4 and Q5 lines from U2015, controls three sections of a quad FET switch, U3025. (RC circuit inputs of each FET control line filter out noise from the digital circuits.) The code is exclusive; i.e., only one FET is switched on at a time. See Table 5-12 for a listing of the codes. When a FET is switched on, it connects a calibration adjustment potentiometer to the summing node of the operational amplifier. Adjustment R1065 sets the 1st LO tune coil sweep, R1071 sets the 1st LO FM coil sweep, and R1067 sets the 2nd LO span.

Table 5-12
CALIBRATION CONTROL SELECTION CODES

U4025		
Pin 3	**Pin 2**	**Selected Adjustment**
low	low	R1065 (main coil)
low	high	R1071 (FM coil)
high	low	R1067 (2nd LO)

Table 5-13
ATTENUATION SELECTION CODES

U2015		
Pin 15 (Q67)	Pin 16 (Q7)	Attenuation Factor
low	low	X1 (K3065)
high	low	X 0.1 (K3075)
low	high	X 0.01 (K4072)

Decade Attenuator

Since accuracy of the digital-to-analog converter is specified as a percentage of full scale, the accuracy decreases as the attenuation is increased. To maintain accuracy at 1%, it is never used at an attenuation factor of more than ten. If more attenuation is required, the decade attenuator, consisting of K4072, K3075, K3065 and the connected divider network, provides further sweep attenuation of X0.01, X0.1, and X1. See Fig. 5-26 for a simplified circuit diagram.

The "2" side of U4025 is controlled by data on the Q6 and Q7 lines from U2015. The "2Y" outputs of U4025 are applied through buffer amplifiers in U4042 to select the appropriate attenuation factor for the output sweep. Table 5-13 lists the states required to energize the attenuation relays. A diode across each relay coil protects the driving circuit from inductive feedback transits.
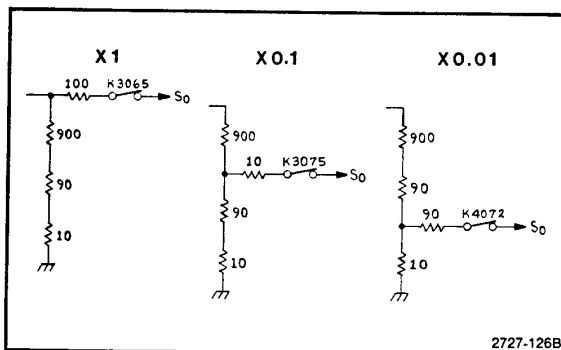

Fig. 5-26. Simplified span decade attenuator.

FIRST LOCAL OSCILLATOR DRIVER
⟨36⟩

Refer to the block diagram adjacent to Diagram 36.

The 1st LO Driver performs the following functions: Buffers the TUNE VOLTS signal and applies it to the dot marker circuit; combines the SPAN VOLTS and TUNE VOLTS signals, and applies the combination to the Preselector Driver. The combined signal is also applied to the Oscillator Driver circuits, which drive the 1st Local Oscillator coils; selects and applies the appropriate tune bias voltage to the 1st Mixer; controls the oscillator filter switch in the 1st LO Driver; produces a stable and precise −10 V reference for both the 1st LO and the Preselector Driver circuits.

The major circuits and their function are as follows:

1) the digital control section buffers the incoming data from the data bus, decodes the address data, selects the required mixer bias, connects or disconnects the TUNE VOLTS and SPAN VOLTS signals for the summing amplifier, energizes the filter switch for the 1st LO, and controls the drive and filtering of the oscillator driver stage;

2) the tune volts buffer buffers the COARSE TUNE VOLTS signal from the Center Frequency Control circuits, and reduces the signal amplitude to drive the dot marker circuits;

3) the oscillator filter driver furnishes drive current to the capacitor switching relay in the 1st LO;

4) the input switching circuits combine the SPAN VOLTS and COARSE TUNE VOLTS signals, and applies these signals to the summing amplifier;

5) the summing amplifier furnishes the drive signal to the oscillator driver. The summing amplifier sums the SPAN VOLTS ramp signal from the span attenuator with the coarse tune voltage from the Center Frequency Control circuit. In less than maximum span, a sweep voltage of ± 10 V sweeps the oscillator at a rate of 333 MHz/division. As the TUNE VOLTS signal varies from −10 to +10 V, the oscillator's center frequency is moved over its full range of 2.072 to 6.35 GHz, plus about 50 MHz overtune at each end;

6) the oscillator driver furnishes swept current drive to the 1st LO coil;

7) the reference supply, which produces a precise −10 V reference for the Preselector Driver and 1st LO Driver;

8) the mixer bias driver produces the required bias voltages for the 1st Mixer in the IF stages.

Digital Control

The digital control circuit sets the oscillator span volts, the 1st Mixer bias and programmable bias for the 492P. Decoder U4034 output Y1 (pin 14) goes low when input address is 72 and output Y7 goes low for address 7E. When either of these outputs go high, data is clocked or latched into U4017, U4024, and U4022. Data for U4017 consists of control codes for the oscillator drive circuits and switch U1016 which selects 1st Mixer bias for the 3.0 to 21 GHz bands, and the bias set by the front panel PEAKING control. The codes are described where each applies to the description and in Table 5-14. Data for DAC U3022 is converted to an analog signal which provides the Programmable Bias for

the 492P. The resistance between output terminals 16, 2, and 15 of U3022 is the input resistance for operational amplifier U2018. R2022 is the feedback resistance.

Tune Volts Buffer. The tune volts buffer consists of amplifier U1025B and surrounding components. The COARSE TUNE VOLTS signal from the Center Frequency Control circuits is reduced to approximately 25% of its amplitude by divider R1028/R1027. The reduced voltage is applied to U1025B, which is configured as a voltage follower with a gain of +1. The output is then fed to the Dot marker stage in the Crt Readout circuits.

Input Switching. This stage consists of FET Q2033, comparators U3014A and U3014C, and FET Q2026. When maximum span is selected, line Q8 of U4017 goes low, causing U3014C to switch. This in turn causes Q2026 to conduct and place R2030 in parallel with R2031, increasing the stage gain of U2032. Also, the same low state is applied to the input of U3014A, which switches and cuts off Q2033. This action disconnects the TUNE VOLTS signal from the amplifier; the TUNE VOLTS is then used only to position a marker on the display. With only the span voltage connected, however, the oscillator is still able to sweep over its full frequency range. The center frequency is equal to the center of the range, which is 4.211 GHz.

If the main coil is not to be swept, line Q7 of U4017 goes low, which cuts off Q3028 and de-energizes K2028. This removes the SPAN VOLTS signal from the amplifier. Diode CR3031 protects Q3028 from the inductive feedback surges that occur at turn-off.

Oscillator Filter Driver. This circuit consists of Q2029 and related components. When relay K2028 is de-energized, as just described, Q2029 conducts. This stage drives a capacitor-switching relay on the 1st LO Interface board. The capacitors are switched across the main coil whenever it is not being swept, to filter noise from the tuning current. Ca-

pacitor C2025 maintains current through the relay after power is turned off, until the coil current has decayed.

Summing Amplifier. This operational amplifier circuit consists of amplifier U2032, complementary pair Q2035/Q2039, and related components. The feedback resistance for this circuit is R1038. The input resistance is R2027 for the COARSE TUNE VOLTS input and R2031 for the SPAN VOLTS input. (R2030 is switched across R2031, as mentioned earlier, to increase stage gain for maximum span operation.) The output of the summing amplifier, which swings from −10 V to +10 V, is applied to the Preselector Driver circuits and to the Video Processor. It is also fed through R1031, the 1st LO SENSE adjustment, summed with the offset voltage from R1032 (1st LO OFFSET), then applied to the source of Q2040. Adjustments R1031 and R1032 match the oscillator driver stage to the oscillator characteristics. R1032 adds offset to the output of U2032 to place the oscillator at center operating frequency when the output of U2032 is at zero volts. R1031 matches the sensitivity of the oscillator to the output amplitude from Q2039/Q2035.

FET Q2040 is used to disconnect the signal from the driver stage. In order to degauss the oscillator coil, (thus establishing a known magnetic history), the microcomputer causes line Q6 of U4017 to go high for about 200 ms. The output of comparator U3014D goes low, cutting off Q2040. This removes all drive from the oscillator coil until the Q6 line returns low.

Oscillator Driver. The oscillator driver stage consists of operational amplifier U2043/Q3047 and surrounding components. It converts its voltage input into the current drive required by the oscillator main tuning coil.

Preamplifier stage Q2045, which receives the signal from the operational amplifier U2032, Q2039/Q2035 through Q2040, is a low-noise matched dual transistor. Q2045 is

Table 5-14
U4017 (U3027) OUTPUT LINES

	Low	High
Q1	Bias 1 connected	Bias 1 disconnected
Q2	Bias 2 connected	Bias 2 disconnected
Q3	Bias 3 connected	Bias 3 disconnected
Q4	PEAKING connected	PEAKING disconnected
Q5	Output Filter disconnected	Output Filter connected
Q6	Driver Input connected	Driver Input disconnected
Q7	SPAN VOLTS disconnected	SPAN VOLTS connected
Q8	Maximum span; TUNE VOLTS disconnected	Normal span; TUNE VOLTS connected

part of the input circuit of a feedback amplifier containing U2043, Q3047, and driver transistor Q352. The feedback path through R3040 and R2042 sets the voltage across a four-terminal resistor R1040. This voltage in turn sets the current of the resistor which is also emitter current for driver transistor Q352. The oscillator coil current 1st LO Sense adjustment R1031 sets the voltage gain of the amplifier which changes the current drive to the oscillator coil.

Capacitor C3038 filters noise on the tune volts and voltage reference inputs. Because of its effect on tuning speed, the capacitor is in the circuit only in the phase-locked mode with phaselock switched off, or when the phaselock option is not included in the instrument. Normally Q5 of U4017 is low, which through U3014B, causes Q3042 to cut off.

Reference Supply. Operational amplifier U2052 and surrounding circuitry form the −10 V reference supply. One side of preamplifier Q2052, biased by R1055 and VR1051, sets a reference voltage at the inverting input of U2052. The output voltage is set by R1034, the −10 V adjustment. U2052 senses changes in load that are amplified by Q2052, and changes the current through regulator transistor Q2051. The diode network across the base-emitter junction, limits the collector current to about 23 mA, protecting the transistor from damage.

Mixer Bias Driver. The mixer bias driver circuit, which consists of quad FET switch U1016, amplifier U1025A, and buffer Q2025/Q1028, plus associated circuitry, furnishes the required bias current (up to 20 mA) to the 1st Mixer circuit. The bias voltage varies from +1 V to −1 V for the internal mixer, and from +1 V to −2.25 V for an external mixer.

Regulator U1013/U1018, provides regulated +12 V and −12 V across the three bias adjustment potentiometers, R1013, R1026, and R1022. The voltage at the center arm of one of thse potentiometers, or the output of U2018, (which represents the front panel PEAKING control setting or programmable bias) is selected by quad FET switch U1016 and applied to the input of U1025A. Quad FET U1016 is controlled by Q1 through Q4 lines from data latch Q4017. A low at any one of these outputs causes the associated FET to conduct and connect that line to the input of U1025A. U1025A drives a pair of transistors, Q1028/Q2025, connected as a complementary pair to provide the 1st Mixer bias voltage.

Programmable Bias. When the microcomputer sends address 7E to decoder U4034, pin 7 (output Y7) goes low. At the end of data output cycle, data is clocked into either U4024 or U4022, depending on which latch is enabled by DB6 or DB7. This data is then converted to an analog current by U3022 which is the current source for operational amplifier U2018. The output of U2018 is a bias voltage that

is fed to either the Preselector Driver board where it is summed with the drive voltage for the Preselector; or, it is fed through U1016/U1025A, and Q1025/Q2025 to the 829 MHz Diplexer, then through RF circuitry to the 1st Mixer or external mixer port.

Oscillator Collector Supply. This circuit comprises amplifier U4055, buffer Q3049, and surrounding circuitry. U4055 holds Q3049 in saturation, so the collector of the transistor remains at a fraction of a volt below +15 V. This voltage is applied to the 1st LO circuits.

PRESELECTOR DRIVER <37>

The Preselector circuit, part of Option 01, provides input selectivity that reduces spurious responses between 1.7 and 21 GHz. Refer to the block diagram adjacent to Diagram 37. The Preselector Driver furnishes the drive current that operates the Preselector Coil, depicted on Diagram 12. It also furnishes a voltage proportional to frequency through the rear-panel ACCESSORIES connector for an external unit. The circuit also drives the relay that selects the preselector or low-pass filter. The Preselector Driver consists of the following major circuits:

1) the digital control circuit, which stores and decodes the data from the microcomputer and control the other parts of the Preselector Driver. The digital control circuit applies the SPAN VOLTS signal to the oscillator voltage processor when FM coil spans are selected; select the gain of the oscillator voltage processor; turn off the drive signal to the current driver for degauss cycles or when the preselector is not in use; select the IF offset voltages to be combined with the FINE TUNE VOLTS signal; add noise filtering at the driver output when the preselector is not being swept; and control the filter select switch;

2) the oscillator voltage processor, which attenuates and offsets the input signal for application to the summing amplifier;

3) the IF Offset stage, which applies an offset voltage to the summing amplifier that is proportional to the IF frequency in use, and to the fine tuning frequency changes of the 2nd Local Oscillator;

4) the summing amplifier, which combines the effective oscillator frequency voltage and the IF Offset voltage, and drives the tracking adjustment circuits;

5) the tracking adjustment circuit, which compensates for different preselector sensitivities, compensates for IF offset and any preselector offset, and compensates for non-linear operation caused by magnetic saturation of the Preselector;

6) the final driver stage, which changes the applied voltage signal into a current drive signal for the preselector coil;

7) the preselector switch driver, which drives the filter select switch, depicted on Diagram 12. The switch requires a positive pulse to select the lowpass filter and a negative pulse to select the Preselector.

Digital Control Circuits

The microcomputer interface circuits, which exercise digital control of the preselector driver circuits, consist of address decoder U5036 and latch U5031. Both the write address, 77, and the read address, F7, are decoded by U5036.

U5031 latches the eight bits of data from the microcomputer on the trailing edge of the DATA VALID signal. This event coincides with the rising edge of the pulse on pin 3 of U5036. Table 5-15 lists output lines from U5031.

The read address function is used by the microcomputer to determine if the instrument is equipped with Option 01. When address F7 is specified, the Y7 line of U5036 goes low. This pulls data line D4 low, informing the microcomputer of the option status.

Oscillator Voltage Processor

The oscillator voltage processor consists of U1101A, U2028, and related components. The signal from the 1st LO Driver is applied to the voltage divider and scaling network formed by R1022, R1021, R1024, and R1031. The purpose of the network is to attenuate and offset the input signal as follows: The input voltage is ±10 V, centered about 0 V, which corresponds to an oscillator frequency of 2.072 to 6.35 GHz. This voltage is the summation of the sweep and tune voltages, with appropriate scaling. The output of the voltage processor is about −1 V at 2.072 GHz to about −3 V at 6.35 GHz, which corresponds to a scale factor of 2.1 GHz/volt. The voltage is directly proportional to frequency; thus the offset is such that if the oscillator could operate to 0 Hz, the voltage processor output would be at zero volts at the same time.

Since the preselector drive input is not swept by the 1st LO Driver when FM Coil spans are used, the sweep must be summed in by this stage. Line Q4 of U5031 moves low when FM coil spans are selected; this causes Q1011 to conduct, which in turn causes Q1022 to conduct. The span volts signal is connected to the inverting input of U1011A, where it is inverted, then applied to the input of U2028.

U2028, as directed by the microcomputer, multiplies the input signal by one or three to transform the input signal to represent effective oscillator frequency in bands 4 and 5 when the 3rd harmonic of the LO is used. When the Q1 line of U5031 is low, the output of one section of quad comparator U5022 is also low, holding FET Q2024 cut off. U2028 is now a unity-gain, non-inverting amplifier. However, when the Q1 line moves high, Q2024 turns on, connecting a resistive network across the amplifier to increase gain by a factor of three. X3 Gain adjustment R1052 sets the gain for precisely three times unity in the tripler mode.

IF Offset Section

The −10 V reference supply, depicted on Diagram 36, furnishes the precise reference voltage for the IF offset circuits. Since the offset voltage is proportional to the IF minus 2.072 GHz, no offset is required for the +2.072 GHz IF. FET Q2034 adds the +829 MHz network into the circuit and Q2036 adds the −829 MHz network. Lines Q7 and Q8 control the two switches by way of quad comparator U5022. One or the other, but not both transistors can be switched on at once; the offset voltage is applied to the inverting input of U2045. At the output of this amplifier, −9 V corresponds to (−829)−2072 MHz, which equals −2901 MHz.

Table 5-15
U5031 OUTPUT LINES

	High	Low
Q1	Selects X1 gain for U2028.	Selects X3 gain for U2028.
Q2	Not used.	Not used.
Q3	Connects tracking adjustment output to final driver stage.	Disconnects tracking adjustment output from final driver stage.
Q4	Connects SPAN VOLTS signal to U1011A input for FM coil spans.	Disconnects SPAN VOLTS from U1011A.
Q5	Selects Lowpass Filter.	Selects Preselector.
Q6	Disconnects output filtering.	Adds output filtering.
Q7	Connects −829 MHz offset.	Disconnects −829 MHz offset.
Q8	Connects +829 MHz offset.	Disconnects +829 MHz offset.

REV AUG 1981

The FINE TUNE VOLTS signal from the Center Frequency Control circuits, which is used to tune the 2nd Local Oscillator, is applied to the input of U2047. Since it is applied here, this makes the fine tune voltage independent of the voltage tripling action in the voltage processor section. The tuning voltage is also applied to the input networks of U2045. Thus, by varying the magnitude of signal in the inverting path compared to the direct path, the proper magnitude and polarity of fine tune offset for each IF offset is provided in the preselector drive signal. Table 5-16 lists the offset voltage required for each frequency band.

Summing Amplifier

The effective oscillator frequency voltage from U2028 and the offset IF voltage from U2045 are applied to the inverting input of U2047. This stage drives the tracking adjustments stage and furnishes a signal for external preselector drive circuits as well. The external drive line has its own return to reduce ground loops.

Tracking Adjustments

These circuits consist of gain-setting offset and shaping circuits. R1065 (PRE-SEL SENSE) is used to compensate for sensitivity variations between preselector stages. R1064 (PRE-SEL OFFSET) is used to compensate for the offset introduced in previous circuits and for any offset in the preselector. This adjustment sets the preselector frequency to 2072 MHz when the output of U2047 is at zero volts.

The four other adjustments (R1054, R1056, R1061, and R1063), are part of a shaper network. The network compensates for magnetic saturation in the preselector, which would cause a deviation from linearity at frequencies above 14 GHz. Each shaper network is switched in by a resistive divider that, at a given frequency, forward-biases the diode in the shaper to shape the current output. Thus, the diodes compensate for the non-linear action of the YIG tuning.

The front panel PEAKING control applies a small offset through R5065 to the input of the current driver stage. This corrects for non-linearity or temperature drift in the 1st LO or Preselector.

Current Driver

This stage consists of output stage Q5065/Q5052; FETs Q3061, Q3077, and Q2074; amplifiers U2054 and U3054; and transistor Q4037.

FET Q2074, as controlled by the Q3 line of U5031, is turned off to reduce the coil current to zero when the preselector is not in use, or during a degauss cycle. During normal operation, the transistor is conducting.

Preamplifier U2054 reduces the temperature drift of the output stage. Driver offset adjustment R2066 nulls the offset voltage, at which point the temperature drift is least. U2054 drives U3054, the main operational amplifier. FET Q3061 isolates U3054 from the output driver.

Current amplifier Q5052 drives the main preselector driver transistor, Q5065. The stage is biased so current flow divides with most of the current going through the output transistor, and a small portion flows through the bias circuits. The currents rejoin at the preselector coil. Resistor R4049 has four terminals; one set carries the coil current, the other set senses the voltage and thus the coil current.

When the preselector is not being swept, line Q6 is low, which causes Q4037 to conduct. This causes Q3077 to conduct, placing C4071 across the Preselector coil. The capacitor reduces noise at the output.

Preselector Switch Driver

Operational amplifier U1011B and the complementary pair of transistors Q4025/Q3025, form the preselector switch driver. This circuit drives the latching relay that is depicted on Diagram 12. This relay requires a positive pulse to select the low-pass filter, and a negative pulse to select the preselector.

Table 5-16
PRESELECTOR FREQUENCY BANDS

Band	Frequency Range	IF	Harmonic	Approximate Voltage Offset
2	1.7—5.5 GHz	−829 MHz	1st	9.0 volts
3	3.0—7.1 GHz	+829 MHz	1st	3.9 volts
4	5.4—18.0 GHz	−829 MHz	3rd	9.0 volts
5	15.0—21.0 GHz	+2.072 GHz	3rd	0 volt

When the Q5 line of U5031 goes high, a positive pulse of about 100 ms in duration, generated through RC network C3021/R3021, appears at the input of U1011B. The output of the operational amplifier drops to about −12 V, and a positive pulse is passed through the transistor pair, selecting the lowpass filter. When the Q6 line goes low, a negative pulse of the same duration is passed to U1011B. The amplifier output rises to about +12 V, and a negative pulse is passed through the transistor pair to select the preselector.

When the circuit is quiescent, neither Q3025 nor Q4025 conduct, since the sum of the zener voltages of VR3011 and VR3012 is greater than the combined supply voltages. When the output of the operational amplifier comes near one of the supply voltages, the transistor that is connected to the other supply becomes saturated, furnishing the necessary drive current to the relay coil. CR4012 and CR4013 protect the driver transistors from induced voltage surges; C3028 and R3028 dampen any oscillation that might occur in the coil circuit.

SWEEP SHAPER AND BIAS CIRCUITS ⟨38⟩

Refer to the block diagram adjacent to Diagram 38. The circuit fundamentally consists of a positive and negative bias supply and a non-linear amplifier that drives the Cavity 2nd LO. The bias circuits supply the oscillator with stable, re-regulated voltages to minimize oscillator FM'ing. The shaper amplifier and diode-resistor arrays combine the FINE TUNE VOLTS and 2nd LO SWEEP signals to form a non-linear driver signal to control the oscillator frequency. The Cavity Oscillator generates the 2182 MHz signal that is used in the 2nd Converter circuits.

Bias Supplies

+12 Volt Regulator. U2047 is a refrence zener diode that furnishes a precise, low-noise temperature stabilized, reference of +6.95 V to the +12 V, −12 V, and +90 V supplies. This voltage is applied through a filter network to the non-inverting input of amplifier U3051, which drives series-pass regulator transistor Q2065. Changes in the output voltage at the emitter of this stage are coupled back to the inverting input of U3051, amplified, and used to restore the output to the original value.

−12 Volt Regulator. Except for the components and the polarity, the plus and minus 12 V supplies operate the same. Refer to the above description for information regarding −12 V supply operation.

+7.7 Volt "C" Regulator. This circuit consists of emitter follower Q3035 and related circuitry. It furnishes a regulated +7.7 V to the Cavity Oscillator. This voltage is derived from the regulated +12 V. The operating bias for Q3035 is set by the voltage divider in the base circuit, which fixes the emitter voltage at +7.7 V.

−8.2 Volt "E" Supply. This circuit consists of comparator U3025, emitter followers Q4026 and Q4024, and surrounding circuitry. Part of the function of this circuit is to ensure that the "C" supply voltage is applied to the Cavity Oscillator first, before the "E" supply. This makes sure that the Cavity Oscillator is excited into oscillation at turn-on.

When the analyzer is turned on, the output of U3025 is clamped at approximately +14 V, because the "C" supply voltage is less than the +6.95 V reference. The base of Q4024 is at about +0.7 V so the transistor is cut off, and the oscillator receives no current from Q4024. When the "C" supply voltage rises past the +6.95 V applied at pin 3 of U3025, the comparator switches and its output drops to approximately −14 V. This cuts off Q4026, Q4024 is biased on, and the Cavity Oscillator can begin operation.

+90 Volt Supply. The principal components of this circuit are amplifier U1087 and transistor Q1076. The circuit takes the +100 V supply output, filters and re-regulates it, producing a stable +90 V for the shaper amplifier. The +6.95 V reference is applied to the non-inverting input of U1087. This is compared to a sample of the output, which is derived through divider R2087/R1086. The regulated +90 V is taken off the emitter of series-pass transistor Q1076.

Shaper Amplifier

This stage consists of amplifier U3089, amplifier U1010, transistors Q1030 and Q2024, and related circuitry. The FINE TUNE VOLTS signal and 2nd LO SWEEP signal are summed at the input of U3089, converting the dual differential inputs to a single-ended voltage for the next stage. The combined signal is applied to the non-inverting input of U1010, amplified, then applied to the base of Q1030 for further amplification. The collector of Q1030 drives the base of emitter-follower Q2024, which in turn provides the tune voltage to the cavity oscillator, tuning or sweeping the unit, as appropriate. Feedback for the shaper amplifier stage is provided through R2018, R1028, and R1026. The gain of the stage is varied by drawing current away from the feedback path into the diode-resistor arrays, as discussed below.

Diode-Resistor Arrays. U1037, U2037, and associated components form a divider array that controls the gain of the shaper amplifier. The input to the amplifier is a variable dc tune voltage plus a ramp voltage that varies in amplitude as a function of the analyzer span setting. Total input swing is within ±10 V. As the output voltage amplitude increases,

the amount of negative feedback decreases. Each diode in the array is biased to conduct at successive amplitude points, until all are conducting. As each diode conducts, more current is drawn from the feedback loop which increases the gain of the amplifier. The resultant output voltage is a non-linear function of the input of the +15 to +40 V range. This voltage is applied to the varactor diode port (Vv) to tune and sweep the oscillator.

Cavity Oscillator

Refer to the Cavity 2nd LO description in the 2nd Converter section.

CENTER FREQUENCY CONTROL ⟨39⟩

Refer to the block diagram adjacent to Diagram 39. The Center Frequency Control circuits form the electrical interface between the front-panel controls and the converter stages in the 492/492P. The circuit receives digital information and instructions from the microcomputer, and converts it to a coarse and fine tuning voltage that is applied to the other elements of the Frequency Control system.

The Center Frequency Control circuits consist of the following major blocks:

1) the Digital Control circuit, which buffers and decodes the addresses and other data to control the other circuits;

2) the coarse and fine storage registers (latches), which store the numerical bytes that control the DAC (digital-to-analog converter) stages;

3) the coarse and fine DAC stages, which convert the digital inputs from the storage registers into analog current and voltage equivalent values;

4) the coarse and fine track/hold amplifiers, which store the analog output values during the approximation routine, and compare the stored value and the approximated value for the microcomputer;

5) the write-back circuits, which inform the microcomputer when the stored value and the approximated values are equal.

Operating Modes

Some explanation of the design principles of the circuit is required before the operation of the circuit can be discussed. DAC devices are now available that can furnish the resolution required to tune the analyzer in small enough steps. To achieve the necessary amount of resolution, two DAC devices are used in tandem. However, this method can cause some errors and non-monotonic behavior in the overall converter circuit.

To circumvent this problem, the outputs of the tandem DAC units are summed together so that the two units are overlapped by three bits (that is, the MSB of the low-order DAC is weighted equally with the third least significant bit, or 2E-10 bit). The overlap means that the lower DAC will have sufficient range to monotonically tune the output of the converter over the entire range of the analyzer, but only if the proper codes of the lower DAC device can be found. Now, suppose that the tandem DAC is loaded as follows:

Upper order:
    1 0 0 0 0 0 0 0 0 0 0 0
Lower order: 1 1 1 1 1 1 1 1 1 1 1 1

The contents of the devices are shown overlapped to illustrate the bit weighting. Now assume that the low-order device is to be incremented one bit. The MSB of the low-order device must be moved into the high-order device before the low-order device can be incremented. Thus, the two must appear as shown below:

High-order:
    1 0 0 0 0 0 0 0 0 1 0 0
Low-order: 0 1 1 1 1 1 1 1 1 1 1 1

If the high-order device operated with no overall linearity inaccuracy, the operation would now be complete, and the low-order incrementation could occur. However, the DAC device can vary by one LSB of the correct value; Fig. 5-27 illustrates a graph of the best and worst case output instances. Note that even in the worst case, the output may move only once every two or three state changes, but the output is always monotonic and within one LSB of the correct value.
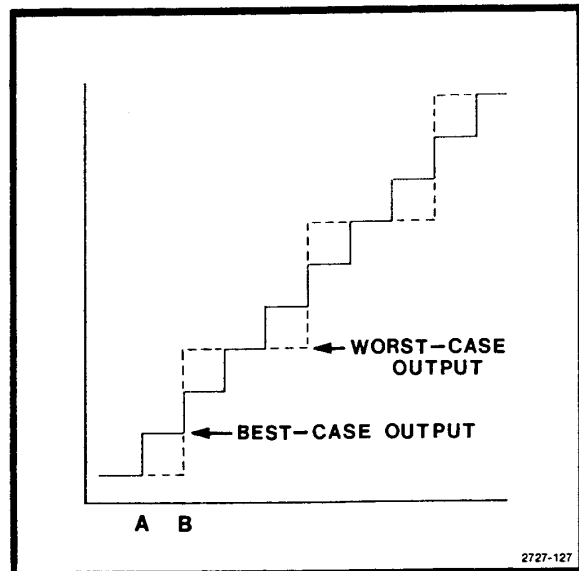

Fig. 5-27. DAC variance graph.

If, in the example shown earlier, the high-order device is at point A in Fig. 5-27, incrementing the device to point B has no effect on the output. If the MSB of the low-order device is set to zero, as shown in the first example, the combined output will actually decrease. Ordinarily, the Center Frequency Control circuit can increment and decrement whenever the microcomputer commands without going through a special routine. However, as just described, some microcomputer adjustment is necessary to compensate for the disparity that usually occurs between the low-order and high-order DAC units.

The first operating mode is the tracking mode, where the preamplifier and integrator are connected together by the disconnect stage, and the entire unit acts as an operational

amplifier. Figure 5-28 illustrates the basic circuit. While the circuit operates in this mode, the amplifier tracks the DAC stage, and sends the voltage out to the tuning circuits.

When the transfer of bits from the lower to the upper DAC is required, the microcomputer commands the circuit to shift to the hold mode. The command comes through the decoder to shut off the disconnect stage, and the preamplifier output is disconnected from the integrator. The integrator holds the voltage that was previously at the output for comparison, and the approximation cycle begins.

The microcomputer resets the low-order DAC to zero. Then, the highest order bit in the low-order DAC is set to
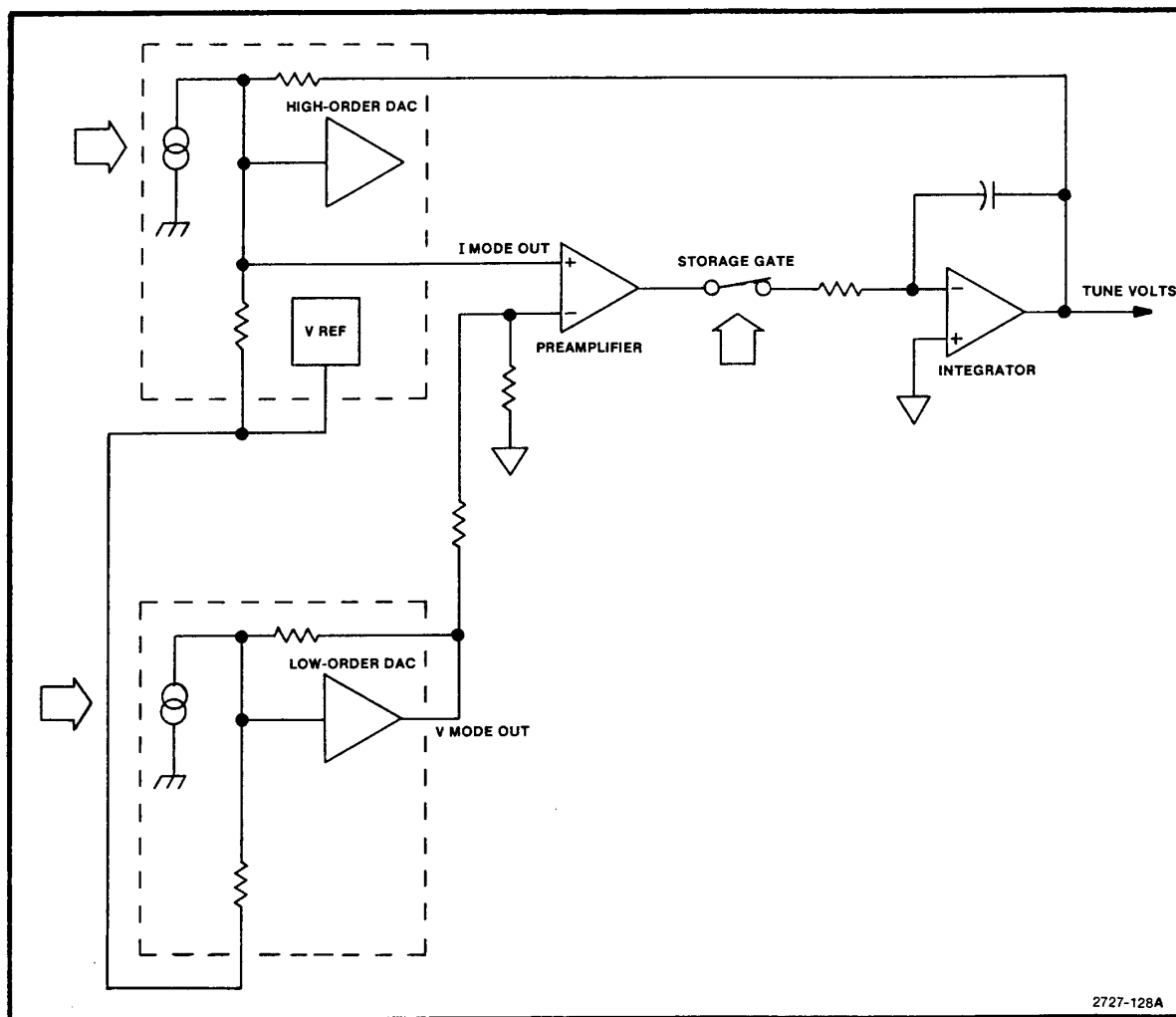

Fig. 5-28. Basic tune voltage converter.

one, and the circuit is queried to find if the DAC output and integrator output is greater or less than required. If less, the microcomputer loads the next lower bit in addition and queries the circuit once more. This process goes on until the two values are the same. Had the microcomputer found that the DAC output was greater than the integrator output at the first inquiry, it would have set the highest order bit to zero and loaded the second-order bit into the low-order DAC, then continued to load successively lower order bits, one at a time, until the circuit signalled that the comparison had reversed. By this process, which is known as the successive approximation method, the circuit finally reaches the point where the outputs are equal, and the microcomputer commands the circuit to shift back to the track mode.

Digital Control

The digital control circuits consist of buffer U2016, address decoder U2014, steering register U2022, and the steering gates (U2024A, U2024B, U2024D, U2026A, U2026B, and U2026C). Because of the quantity of data that must pass through these circuits, a steering register is used that has a separate address. The first byte of data, which is the steering byte, is clocked into U2022 by the ADDRESS 70 signal. The output levels are applied to the steering gates, and the circuit waits for the next byte. The microcomputer then furnishes the first byte of data to be sent to low-order fine-tune digital-to-analog converter DAC, for example, by way of storage register U3022. The byte is clocked into the register by the coincidence of low states at the inputs of U2026C; one from the steering byte, and the other from the ADDRESS 71 signal, which is used to clock the steered data bytes into the correct register. This continues until seven bytes of data have been clocked into the circuits, including the steering byte. The third output from U2014, ADDRESS 80, controls transistors Q2043 and Q1039, which enable the write-back function.

In addition to the six steering lines that drive the steering gates, U2022 also controls, by means of the Q1 and Q8 lines, the hold/track selector transistor for each converter side. Table 5-17 illustrates the format for ADDRESS 70. Addresses are expressed as hexadecimal numbers. Table 5-18 lists some of the significant states that are used to tune the DAC.

Table 5-17
ADDRESS 70 FORMATS

DB0	Fine Tune hold
DB1	Fine Tune low byte enable
DB2	Fine Tune mid byte enable
DB3	Fine Tune high byte enable
DB4	Coarse Tune high byte enable
DB5	Coarse Tune mid byte enable
DB6	Coarse Tune low byte enable
DB7	Coarse Tune hold

Storage Registers. Six storage registers are used in the circuit, (U1014, U1016, U1022, U3014, U3016, and U3022 respectively). Since both sets are identical, only the first three are described.

Data from U2016, the data buffer, is clocked into the registers each time a different tune voltage is required. U1022 feeds the lowest eight bits to the low-order DAC, U1026; U1014 feeds the highest eight bits of the high-order DAC, U1032; and U1016 feeds the remaining bits of both units.

Digital-To-Analog Converters. Each side of the converter has two DAC stages contained on sub-assemblies A46A1 and A46A3, DAC 1200 Interface. These sub-assemblies plug into the Center Frequency Control Board A46 through IC sockets J1024 and J1030 for the Coarse Tune circuit, and J3024 and J3030 for the Fine Tune circuit. Since both sets operate the same, only Coarse Tune units are described. Each DAC furnishes current or voltage outputs that are commensurate with the data applied. Figure 5-28 is a functional block diagram of each DAC, illustrating its operation in the circuit. U1020 is the low-order DAC, U1026 is the high-order DAC. U1012 and Q1018 are configured as an operational amplifier to provide the drive for U1024.

The DAC unit is basically a programmable current generator that drives an internal high quality operational amplifier.

Table 5-18
DAC TUNING CODES

Tuning Point	Data	Address	Results
Positive full-range	00	70	Enables all latches, track mode
	00	71	Loads zeros into all positions of both DAC's
Mid-range	00	70	Enables all latches, track mode
	00	71	Loads zeros into all positions of both DAC's
	33	70	Enables high byte latch, track mode
	80	71	Loads 80 into DAC's. Midrange value
Negative-full-range	00	70	Enables all latches, track mode
	FF	71	Loads FF into all positions of both DAC's

In this configuration, only the low-order DAC uses the internal operational amplifier. Thus, the low-order unit operates in the voltage output mode, and the high-order unit operates in the current output mode. The two devices feed the two inputs of preamplifier U1044, which sums the two inputs, amplifies the sum, and sends it through the switching circuit to the integrator.

Since the DAC units generate the dc voltage that tunes the entire instrument, noise and extraneous signals must be kept at a minimum. Thus, each tune voltage is provided with an isolated ground system, U1042A/U1042B for the Coarse Tune voltage converter, and U3041A/U3041B for the Fine Tune voltage converter.

Track/Hold Amplifiers

Since the coarse and fine amplifiers are identical in operation, only the coarse amplifier is described here. The amplifier consists of preamplifier U1044, control transistor Q2044, storage gate FET Q2046, and integrator amplifier U2046.

The output of the low-order DAC (U1024) is fed through input resistor R1048 to the inverting input of preamplifier U1044. The current output of the high-order DAC U1030, is fed directly into the non-inverting input of the preamplifier. Feedback resistor R1044 establishes the gain of the stage at about 10,000 (ratio of R1044 to R1046). The combination of CR1046, CR1045, and R1047 in the feedback circuit, prevents the output from swinging to extreme voltages with large input signals. Thus, whenever the output exceeds about one volt in either direction, one of the diodes conducts and connects R1047 and R1045 across the feedback path to reduce the gain of the stage to about unity. The output signal from the preamplifier is connected to the source of storage gate FET Q2046. The gate of this device is controlled by transistor Q2044. Normally the circuit is tracking, so line Q8 (B7) from U2022 is low and Q2044 is conducting. CR2042 is cut off since the voltage drop across R2043 holds the gate of Q2046 at about −0.3 V. (The −0.3 V back bias on the source-gate junction reduces memory slewing while switching modes.) Q2044 holds the diode back-biased as long as the transistor continues to conduct. This permits Q2046 to pass the signal from the preamplifier output to the integrator input.

Integrator U2046 tracks the preamplifier output during track mode and serves as the inverting amplifier for the feedback system shown in Fig. 5-28. Under normal circumstances the incoming signal is routed through R2046. To improve the amplifier's slewing rate, CR2044 and CR2045 conduct to connect R2047 in parallel with R2046 when signals in excess of one volt are applied. This speeds up the response of the circuit when large scale tuning changes are required.

When the hold mode is selected, line Q8 (B7) of U2022 moves high, Q2044 cuts off and CR2044 pulls the gate of Q2046 low enough to cut off the FET. This disconnects the preamplifier from the integrator which then maintains the charge on C2046 during the approximation routine. COARSE TUNE RANGE adjustment R1032 is connected across pins 16 and 18 of U1030. It compensates for the different resistance values inside the DAC. This variation is more serious in the higher-order DAC owing to its greater effect on the output.

Write-Back Circuits

These circuits consist of amplifier U2044 and U3045, plus enabling transistors Q1039 and Q2043. Since both are identical, only the coarse circuit is described.

Following the command to shift to the hold mode, the microcomputer will interrogate the circuit to see if the DAC output and the stored voltage match. It does this by pulling ADDRESS 80 high. This causes Q1039 to conduct, which in turn furnishes U2044 with operating current. The output of U2044 is at zero volts when the two input voltages match. If the loop error voltage is high, U2044 will pull down on DATA BUS line 7. This informs the microcomputer whether the bit just set is too large or too small. The output of U2044 is open-collector, so it has no effect on the data line when it is not pulling the line low.

<div align="center">◇8◇</div>

PHASELOCK SYSTEM
(Option 03)

Functional Description

The phaselock section, which is included when Option 03 is part of the instrument, is a frequency control system that substantially improves the stabilization of the 1st LO (first Local Oscillator).

The phaselock system consists of two frequency servo loops, called the outer loop and inner loop. Operation of the inner loop is as follows: The 100 MHz reference signal from the 3rd Converter is applied to the Synthesizer, where it is first divided by two, then sent to the phaselock circuits to be used as a reference frequency. It is further divided to 25 MHz in the synthesizer circuits and applied to the ÷ N circuits which reduce the signal to a reference frequency (depending on the ÷ N number), between 32 and 94 kHz and applied to the Offset Mixer, where it is compared with the mixer output. The original 25 MHz is also applied to the Offset Mixer.

The Controlled Oscillator operates between 25.032 and 25.094 MHz, depending on the drive from the Error Amplifier. This signal is applied to the Offset Mixer, where it mixes with the 25 MHz reference frequency. The difference frequency, which is from 32 to 94 kHz, is applied to the phase/frequency detector and compared to the ÷ N reference frequency. If the two signals are edge and frequency coincident, phaselock occurs. If they do not coincide, an error signal is generated, passed through the Error Amplifier, and applied to the Controlled Oscillator. This forces the oscillator to shift to the reference frequency. This evolution typically lasts for only a few milliseconds, so the inner loop phaselock is, for all practical purposes, instantaneous.

The outer loop, which includes the inner loop circuits (Offset Mixer, Error Amplifier, and Controlled Oscillator), consists of the Strobe Driver, Phase Gate, Error Amplifier, and 1st LO. (The phaselock control circuits are a part of the operation, but are not considered a part of the loop.)

The 25.032 to 25.094 MHz output from the Controlled Oscillator is applied to the Strobe Driver, where it is divided by five, filtered, and sent to the Phase Gate Detector as a 5.006 to 5.019 MHz strobe signal. This signal generates line spectra that are equally spaced about 5 MHz apart over the entire spectrum (at about the 400th line, which corresponds to about 2 GHz). Assuming that the 1st LO is tuned in that vicinity, one of these lines is within 2.5 MHz of the 1st LO frequency. The Phase Gate outputs a signal that is proportional to the difference between the 1st LO frequency and that of the nearest strobe line. The signal is counted by the phaselock control circuits.

Now, as the search for phaselock begins, the microcomputer moves the strobe in about 1 MHz increments. It does so by sending a new number for each step to the ÷ N Counter. With each change in the ÷ N output signal, the Controlled Oscillator frequency changes to match, and the strobe signal shifts toward the 1st LO frequency. When the Phase Gate generates an error that is below 500 kHz, it passes through the filter in the Error Amplifier circuits, and the microcomputer is notified of the proximity of the strobe. The microcomputer now backs the strobe away from the 1st LO frequency in smaller increments until the 500 kHz bandwidth is encountered. This locates the 1st LO to be about 500 kHz away from the strobe signal. The microcomputer now moves the strobe to the middle of the bandwidth, about 250 kHz away, then takes three small steps closer while noting the change in error frequency with each step. With this information, the microcomputer can compute the position of the 1st LO frequency, does so, and places the strobe within approximately 10 kHz of the 1st LO frequency. Then, the microcomputer commands "lock", which puts a more precise servo system into operation, as follows.

Previously, the microcomputer was moving the strobe around to find coincidence with the 1st LO frequency. The F(s) amplifier in the Error Amplifier circuits will now change the current to the FM Coil of the 1st LO so the 1st LO frequency finds and locks on frequency with the strobe. Any frequency difference between the strobe signal and the 1st LO will generate a correction voltage of low frequency that is filtered by the F(s) amplifier, then used to drive the FM Coil back to the strobe position. If the 1st LO drifts beyond the operating range of the F(s) amplifier, the microcomputer is alerted and the remainder of the circuits indicate the direction of drift. The microcomputer then tunes the Center Frequency Control circuits to null out any FM coil current in the phaselock loop.

PHASELOCK CONTROL 〈40〉

Refer to the block diagram adjacent to Diagram 40.

The Phaselock Control section consists of the following major circuits:

1) the address decoder, which receives and decodes the talk and listen commands for the phaselock loop;

2) the service request circuits, which sense an impending loss of phaselock, send a service request to the microcomputer, and cancel the request when directed by the microcomputer;

3) the data buffer, which transmits and buffers data from the microcomputer to the phaselock control and inner loop circuits;

4) the multiplexer divider circuits, which multiplex input signals, including the F ERROR signal, and divide the signal frequency for application to the counter-buffer stages;

5) the counter buffer, which accumulates the divided signal from the multiplexer-divider circuits; then, upon command from the microcomputer, multiplexes the data from the buffers to the data bus. Some status signals share one of these buffer stages;

6) the phaselock sensor circuit, which monitors the SEARCH signal, and informs the microcomputer of phaselock status.

Address Decoder

The addresses from the microcomputer are decoded by decoder U7055. The phaselock control circuits have both a talk address, where the counter-buffer circuits are instructed to talk on the data bus, and a listen address, where U7041 is directed to receive data from the data bus. The talk address is F3; the listen address is 73.

Service Request Circuits

The service request circuits consist of multiplexer U6105, one-shot U6028B, latch U6066A, and associated circuitry. This circuitry alerts the microcomputer in the event that the 1st LO has drifted too far.

The UP and DOWN signals from the window comparator (located on the Error Amplifier board) drive NOR gate U6015. Both signals are also sent to U4025, where their status can be read by the microcomputer. When one of these signals is high it indicates that the Error Amplifier is approaching its operating limits and the microcomputer should adjust the 1st LO frequency so the Error Amplifier returns to the center of its range. A high at either input of U6015B produces a negative transition that triggers one-shot U6028B. U6028B remains set for about 35 μs and sets U6066A, causing two actions to occur: The Q output drives Q7060 into saturation initiating the service request for this address and the complement output of U6066A pulls the 1G and 2G inputs of multiplexer U6105 low, enabling both sides. This device allows Q4090 and U6066A to respond to inquiries by the microcomputer to determine which address requested service. The microcomputer initiates the polling routine, which consists of pulling the POLL signal and AB7 high, then interrogating each data bus line in succession to determine which requested service; that is, which data line is low. This is done by setting the 1Y output of U6105 high, which causes Q4090 to pull the D2 line low. To affirm which address requested service, the microcomputer now causes the 7 address line to move low, which, via the 2Y line from U6105, clocks U6066A to the reset state as the microcomputer holds data bus line 2 low. This cancels the service request by cutting off Q7060, permitting its output to move high. In addition, the complement output of U6066A moves high, disabling the inputs to U6105. This brings the service request circuitry back to its original state.

Data Buffer

This consists of buffers U7041, U6078D, U6078A, and U6078E. U7041 is the listen buffer for the Phaselock Control circuits. When address decoder U7055 is addressed to listen by the microcomputer it enables U7041, which passes on the buffered data to the other circuits in the Phaselock Control and inner loop circuits. The function of each data bits is as follows:

D0   This line carries the data that preloads the ÷ N counter in the synthesizer circuits bit by bit in serial format.

D1   The N LATCH signal is sent on this line. It is used to latch the N DATA into the synthesizer counters.

D2   Reserved for future applications.

D3   This signal resets the buffer sequencer at the outset of a talk cycle for the counters.

D4   This line (CONTROL LATCH) latches a control word into the output buffers of U2025 on the Error Amplifier board.

D5   This signal clears all the counter stages in the counter-buffer circuits in anticipation of a count sequence.

D6   By controlling the state of U6066B, this line selects the signal source to be passed through U2105 to be counted.

D7   This line furnishes the clock pulses for two areas of circuitry. First the clock, which starts out coincident with the N DATA on line D0, is delayed by an RC circuit; then, it passes through buffer U6078D where it is sent in two directions. The signal is buffered through U6078E and used as the clock pulse for U6066B. Also the signal, now delayed, is used as the shift register clock for the ÷ N counter latches on the Synthesizer board. The slight delay is to provide adequate setup time for the data prior to the clock signal arriving.

Multiplexer-Divider

This circuit consists of U6078B, U2105, and U2091. The F ERROR signal enters at pin 12 of the board where it is routed through buffer U6078B and applied to multiplexer U2105. This multiplexer selects between several signal sources to be counted. However, all other possible signal sources apply to future applications, so for the time being, U2105 passes to only the F ERROR signal through to U2091. The F ERROR signal enters the multiplexer at pin 4. It is passed through to the 1Y output, and into the upper section of dual four-bit binary counter U2091, where it is divided by two, and sent out the QA output. This signal is passed through the other side of the multiplexer, out the 2Y line, into the lower section of U2091. The QC output of U2091, which is the F ERROR signal divided by eight, is applied to the first counter, U2065. The QD output, which is F ERROR signal divided by 16, is used to control the multiplexer, and to keep the microcomputer posted on the progress of the count.

Refer to Fig. 5-29 which illustrates the timing relationships. The circuit functions as follows. At the outset of a count cycle, the microcomputer sets the D5 line high, to clear all of the counters including U2091. All outputs of U2091 that are connected are low. This enables U2105 to pass signals. At the first negative edge from the F ERROR

U2091 BEGINS COUNT

F ERROR

U2091-9 (QC)

U2065 BEGINS COUNT

U2065 STOPS COUNT
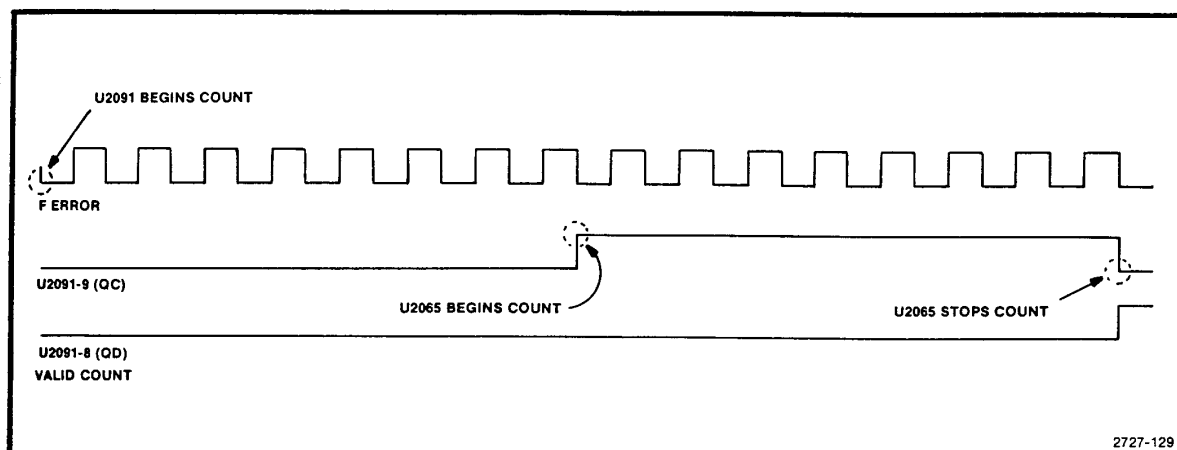
U2091-8 (QD)
VALID COUNT

2727-129

Fig. 5-29. Timing diagram for F ERROR count.

signal, U2091 begins counting. Eight cycles later QC moves high, enabling U2065 to begin counting the buffered 50 MHz signal from the synthesizer circuits, by way of U4014C. The count continues until eight more cycles of F ERROR have occurred, at which time line QD moves high, disabling the multiplexer and stopping the F ERROR signal from passing. The count will remain in the counters until it is cleared by a command from the microcomputer.

Counter-Buffer Stages

This circuit consists of counters U2065, U4062, and U2055; buffers U4049, U2036, and U4025; buffers U6015A and U4074B; and the buffer multiplexer, which consists of counter U2078 and buffer U4074A.

As mentioned earlier, the 50 MHz signal from the Synthesizer is applied to the input of U2065, and the five four-bit stages are permitted to count this signal for the period that U2091, pin 9, remains high. As this occurs, the microcomputer periodically examines the state of the VALID COUNT line. It does so by resetting U2078 through data sent through U7041; when U2078 is reset, pin 3 is high. When the microcomputer pulls the Y7 line of U7055 low, the outputs of U4074A are enabled, which in turn enable the outputs of buffer U4025. These output lines are connected in common to the output lines of the other two buffers, but neither of the others are enabled, so they have no effect for the present. The microcomputer is thus able to examine the VALID COUNT line; if it is still low, indicating that the count is not complete, the microcomputer releases the Y7 line, which increments U2078 and disables U4074A. This in turn disables all three buffers and clears the data bus. If the VAL-ID COUNT line is high when the microcomputer interrogates the stage, the data from U4025 is accepted; the microcomputer then re-addresses U7055, which increments U2078, and U2036 is enabled instead of U4025. The

microcomputer accepts that data, then once more increments U2078. This enables the last of the three buffers, U4049, to send its data on the bus. When the microcomputer receives the last of the three data bytes, it resets U2078 and clears the bus.

Phaselock Sensor Circuits

This circuitry consists of transistors Q7030 and single-shot U6028A, plus surrounding circuitry. The SEARCH signal from the Error Amplifier is applied to Q7030 for amplification, then applied to trigger the one-shot U6028A. The period of the SEARCH signal (when the 1st LO is not phaselocked) is shorter than the time constant of U6028A so the single-shot cannot return to its quiescent state. Thus when the microcomputer examines the D4 line, it is informed that the circuits are still in search condition and that phaselock has not yet occurred. When the instrument finally enters phaselock, the error amplifier stops oscillating (i.e., searching for a lock point), U6028A times out to the reset state, and the LOCK line from U6028A moves high. When the microcomputer later interrogates the board, it will be informed that the instrument is in phaselock. Also when the single-shot times out, Q5030 is cut off, permitting the UP and DOWN lines to move freely so that the service request circuits are once again in operation.

ERROR AMPLIFIER AND SYNTHESIZER
⟨41⟩ ⟨42⟩

The Synthesizer uses the 100 MHz reference frequency from the 3rd Converter to generate 50 MHz for the

Phaselock Control, and 25 MHz plus a ÷ N frequency, determined by the ÷ N number, for the Offset Mixer. The ÷ N number produced by the Synthesizer, is determined by the microcomputer and ranges from 32 to 94 kHz.

The Error Amplifier:

1) integrates the error signals from the Offset Mixer and produces a correction voltage to pull the Control Oscillator to a frequency that is synchronous with the ÷ N signal;

2) generates a STROBE ENABLE to enable the strobe generator in the Strobe Driver circuit;

3) produces an UP or DOWN signal to alert the microcomputer that the drive current to the 1st LO FM coil is reaching its limit in holding the 1st LO in phaselock;

4) generates an F ERROR signal, from the outer loop ERROR 1 signal, to be used by the Phaselock Control in determining the proximity of the 1st LO frequency to the strobe line.

Synthesizer Circuits

The Synthesizer can be divided into the following functional blocks: the 100 MHz divider, the 50 MHz divider, and the ÷ N counter.

100 MHz Divider. This circuit consists of flip-flop U3030, and differential pair Q3040 and Q3041. The 100 MHz signal from the 3rd Converter stage is applied to the clock input of U3030. (One-half of U3030 is used to furnish a stable bias source for the clock input.) The signal from the Q output is applied to Q3041, from which it is sent to the Phaselock Control circuits. The signal from the complement output of U3030 is applied through Q3040 to U1040B, the 50 MHz divider.

50 MHz Divider. This circuit consists of U1040B. The 50 MHz from the collector of Q3040 is applied to the clock input of flip-flop U1040B which divides the signal to 25 MHz. The signal from the Q output is sent to the Offset Mixer circuits. The complement signal is applied to the ÷ N Counter.

÷ N Counter. This stage consists of two shift register/latches U2020 and U2030; three counters, U2010, U1020, and U1030; and flip-flop U1040A. The circuit is controlled by three signals from the microcomputer by way of the Phaselock Control circuits. The ÷ N Counter is used to furnish the 32 to 94 kHz reference frequency, which is applied to the Offset Mixer circuits. When power is first applied, and before phaselock is selected, this counter typically operates at about 6 kHz.

When phaselock operation is selected, the microcomputer sends data and a data clock to load a number into the latches, which accept and store serial data. The numbers that come from the microcomputer range from about 3300 to 3830, so the count remaining, until the counters overflow, is from about 265 to 795. When the number is loaded, the N LATCH signal transfers the number from the input shift registers to the output registers of U2020 and U2030 where they are available to the counter stages. This presets the counters to a predetermined value, as just mentioned. Once loaded, the counters count at a 25 MHz rate to accumulate the remaining number of digits until they are full. Then the TC output of U1030 moves high and U1040A changes state. This presets the N number in the counter stages for another count cycle. The TC output of U1030 is again simultaneously set low so the next cycle of the 25 MHz clocks U1040A back to the reset condition. The resultant output of U1040A is a series of positive pulses that range in period from 10 μs to 31 μs which is equivalent to 94 to 32 kHz. This signal is sent to the Offset Mixer for comparison with the difference frequency generated in the mixer circuit.

Error Amplifier

The Error Amplifier circuits consist of the digital control circuits, which decode the data from the microcomputer to drive other circuits on the board; the inner loop error voltage amplifier, which furnishes the tune voltage to the Controlled Oscillator; the search amplifier which drives the phaselock sensor circuits on the Phaselock Control board and the FM coil of the 1st LO; the window comparator which drives the service request circuits on the Phaselock Control board; and the error signal filter which filters and squares the ERROR 1 signal from the Phase Gate, and applies it to the multiplexer-divider circuits on the Phaselock Control board.

Digital Control Circuits. These consist of shift register U2025 and quad switch U2037. Data from the microcomputer is fed serially, by way of the Phaselock Control circuits into the shift register, then transferred to the output lines by the LATCH signal. Table 5-19 lists the purpose of the output lines.

Error Voltage Amplifier. This stage, which consists of differential amplifier U3075 (shown on Diagram 41) and surrounding components, compares the outputs of the phase/frequency detector on the Offset Mixer board, furnishing an oscillator tune voltage to the Controlled Oscillator. Refer to the Offset Mixer description that follows for a more detailed description of this circuit.

Table 5-19
U2025 OUTPUT LINES

Line	High	Low
Q1	Window disabled (QS low)	Wide window (QS low)
Q2	Lock (connected FM coil)	Unlock (disconnected FM coil)
Q3	Search (wide loop gain response)	Narrow loop gain response
Q4	Strobe enabled	Strobe disabled
Q5	Narrow window	Wide window (with Q1 low)

Search Amplifier. This circuit consists of amplifier U2048 and surrounding components. The ERROR 1 signal from the Phase Gate Detector and Error Amplifier is applied through LOOP GAIN adjustment R3082 to the inverting input of U2048. The signal (ERROR 1) is a result of the comparison of the 1st Local Oscillator frequency and the nearest multiple of the STROBE signal from the Strobe Driver circuit. The ERROR 1 signal varies from zero to about 500 kHz, and is up to four volts peak-to-peak in amplitude. The LOOP GAIN adjustment is set for best sensitivity with minimum hunting.

Amplifier U2048 is connected to operate as a low-pass filter/integrator for the incoming ERROR 1 signal. During search operation, however, the inverting input side of the amplifier causes the stage to operate as a Wien-bridge oscillator at about 25 Hz. At this point, the U2037 outputs are in the following states: Q1 line is high (contacts open) because the phaselock system is in search mode; Q2 is high (contacts closed, which allows U2048 to drive the FM coil); Q3 is high, allowing the lock bandwidth to be over 100 kHz wide (thus, the Wien-bridge circuitry has sufficient positive feedback to oscillate); Q4 is high, which enables the strobe; and Q5 is low because the system is in search mode. (Q1 and Q5 remain open during this part of the search operation to hold the window comparator disconnected.)

As the Strobe signal frequency is changed to be nearer the 1st LO frequency, the ERROR 1 signal decreases in frequency. Since the inverting side of U2048 is a low-pass filter, the decreasing frequency receives more amplification, until enough feedback occurs on the inverting side to suppress the oscillations on the non-inverting side (i.e., the negative feedback exceeds the positive feedback that normally sustains oscillations).

The SEARCH signal (once locked) is now essentially a dc level so the Phaselock Control circuits indicate to the microcomputer that lock has occurred; it in turn causes line Q3 to move low, closing the feedback path for the inverting side of U2048. This decreases the bandwidth, ensuring that the amplifier cannot break into oscillation until phaselock is broken. It also improves the close-in noise performance of the phaselock loop.

Window Comparator. This circuit consists of U1015 and the associatd components, and is used to sense when U2048 has approached its operating limits. When the microcomputer causes the Q2 signal to close the path from U2048 to the FM coil, U2048 begins to furnish current to the coil which causes the 1st LO to track the stable strobe signal. That is, each time the 1st LO frequency drifts, the ERROR 1 signal changes and U2048 shifts the FM coil current to bring the 1st LO back to its original frequency. At the same time, the microcomputer causes lines Q1 and A5 to be low, closing the contacts that connect the output of U2048 to the input of the window comparator through a divider network. Now, as the 1st LO frequency drifts, the search amplifier will compensate for the drift. If the drift is excessive, however, U2048 will approach its design limits and will be unable to furnish any more current to the FM coil.

Window comparator U1015 is a dual comparator stage that senses a deviation of ±15 mV. For instance, if a frequency shift forces U2048 to move positive enough (approximately 3 V), the upper half of the comparator conducts, and the UP line goes high. This triggers the service request circuits on the Phaselock board, which in turn alerts the microcomputer, which then begins adjusting the TUNE voltage from the Center Frequency Control circuits. If the output drifts negative, the other half of U1015 conducts, causing reverse action to occur.

Ordinarily, the input to the window comparator is attenuated by R2043, which reduces the voltage applied to U1015 to 0.3% of the output from U2048. This allows U2048 to drift up and down without immediately triggering either comparator. When R2043 is in the circuit, it is called "wide window" operation. When phaselock is de-selected, the microcomputer selects narrow window (which bypasses R2043). The Center Frequency Control circuit is then instructed by the microcomputer to move the 1st LO frequency until the window comparator indicates that the FM coil current is near zero. This prevents the 1st LO frequency from shifting too far from the lock point when phaselock is cancelled.

Error Signal Filter. This circuit, which consists of active lowpass filter U2065 and Schmitt trigger U1035, filters and

squares the incoming ERROR 1 signal for application to the Phaselock Control circuits. The ERROR 1 signal is applied through C2067 to an RC filter network that is a 500 kHz low-pass filter. After filtering, the signal is applied through ERROR COUNT BREAKPOINT adjustment R1061 to the input of U1035, a Schmitt trigger circuit. The squared output signal is then applied to the Phaselock Control circuits where it is used by the microcomputer for determining the relationship between 1st LO frequency and the strobe line.

CONTROLLED OSCILLATOR, OFFSET MIXER, AND STROBE DRIVER ⟨42⟩

Controlled Oscillator

The Controlled Oscillator is a voltage-controlled crystal oscillator whose frequency is controlled by the output of the Error Amplifier. The oscillator generates a reference signal that is used to stabilize the 1st LO frequency.

Refer to the block diagram adjacent to Diagram 42. The control voltage from the Error Amplifier, which is a function of the difference between the microcomputer controlled ÷ N signal and the Offset Mixer difference frequency, is applied to the Controlled Oscillator to regulate its frequency of operation. The circuit has two outputs: the first, which is part of the inner loop of the phaselock circuits, is fed to the Offset Mixer, where it is used to derive the difference frequency that is compared against the ÷ N signal. The second output, which is part of the outer loop, is fed to the Strobe Driver circuits, where it is divided down to become the STROBE signal that is compared against the 1st LO signal in the Phase Gate.

The Controlled Oscillator consists of five major circuits, four of which are connected in a positive feedback loop to sustain oscillation. These circuits are the resonator stage, the differential amplifier, the bandpass filter, the isolation amplifier, and the output amplifier. The resonator stage operates at a frequency of 25.032 MHz to 25.094 MHz. It presents a high impedance to ground at resonance, which reduces as the operating frequency moves away from the resonant point. The output signal from the resonator is fed to the differential amplifier, which splits the signal and sends it to the output amplifier and the bandpass filter. The output amplifier sends the signal to the Offset Mixer and the Strobe Driver, and reduces loading of the feedback loop. The bandpass filter strips the signal of any spurious responses or harmonics and feeds the signal to the isolation amplifier. This stage furnishes the positive feedback drive to the resonator stage and isolates the bandpass filter from the resonator stage.

The resonator stage consists of crystal Y1012, varactor diodes CR1011 and CR1012, and related components. The stage operates within a frequency range of 25.032 to 25.094 MHz, controlled by the voltage applied to varactor diodes CR1011 and CR1012. Feedback energy for sustaining oscillations comes from the isolation amplifier by way of coil L1025.

The resonator output signal is applied to a differential amplifier Q2033 and Q2041. The Q2033 side drives the output amplifier and serves to isolate the output load from the feedback loop. Gain from this side is less than one. The signal is fed from the collector of Q2041, following amplification, into the bandpass filter.

The bandpass filter consists of passive components, and is used to strip the signal of any frequency components more than about 40 kHz away from the center operating frequency, which is approximately 25.06 MHz. Capacitors C1041 and C1042 are adjusted at the factory to set the bandwidth and center frequency of the filter. The signal from the filter is sent to the isolation amplifier.

Transistor Q1028 and related components make up the isolation amplifier. The amplifier is a common-base configuration, in order to match the impedance of the filter to the resonator. Output current from the stage furnishes positive feedback for the resonator.

The output amplifier consists of transistors Q2025 and Q2026, which are connected as a differential pair. The signal from the collector of Q2026 furnishes the signal that drives one side of the Offset Mixer; the signal from the collector of Q2025 drives the input of the Strobe Driver circuit, for eventual application to the Phase Gate circuits.

Offset Mixer

The Offset Mixer consists of a ring diode mixer circuit, a differential amplifier, and a phase/frequency detector. For explanatory purposes, assume that the Controlled Oscillator frequency is at 25.06 MHz and the ÷ N signal is 50 kHz.

The 25.06 MHz signal from the Controlled Oscillator enters the board at pin N of the Offset Mixer assembly. It is applied to the base of transistor Q2021 which drives transformer T2010. The output of T2010 is connected across the ring diode mixer. The 24 MHz reference frequency is applied at pin K of the Offset Mixer and coupled through T1010 to the ring diode mixer. The four frequency components are picked off at the center tap of T2010. The two fundamental frequencies and the sum are blocked by a pi filter, and the

60 kHz difference is coupled across T2030 to a differential pair Q1020/Q1030, then amplified to TTL levels by amplifier Q1040 and applied to the clock input of flip-flop U1050B, part of the Phase/Frequency detector.

The Phase/Frequency detector consists of flip-flops U1050A and U1050B, NAND gate U2050B, and inverter U2050A. Now, if the loop had been locked, the two flip-flop clock input signals would have been edge-coincident. Pin 4 and 5 inputs of U2050B would have moved high and after the signal at TP1058 goes low, the NAND gate would have reset both flip-flops. The result would have been a series of pulses of equal amplitude and width from each of the flip-flops. This would cause equal voltages to be applied to the Error Amplifier, and the Controlled Oscillator frequency would shift.

It is assumed, however, that the ÷ N signal is 50 kHz and the difference frequency from the collector of Q1040 is 60 kHz, for this description. Thus, the output of Q1040 is leading the ÷ N signal. U1050B sets first placing a high at the inverting input of U3075 which pulls the output of U3075 low until U1050A sets. A short time later, U2050B resets both flip-flops and U3075 will switch back to balance until the next correction cycle. This continues to occur until the two signals applied to the Phase/Frequency Detector are edge-coincident.

The correction voltage in this example from U3075 is applied to the frequency-determining components of the Controlled Oscillator, and its frequency shifts downward. The frequency of the oscillator will continue to decrease until the output of U3075 is stable.

The Error Amplifier, which is part of the Error Amplifier assembly, is described here because it is an integral part of the inner loop. The stage consists of differential amplifier U3075 and surrounding components. As the signals driving the amplifier continue toward one direction, U3075 continues to drive the oscillator down in frequency. The circuit consisting of VR2065, CR3069, R2067, and C2072 clamps the output to prevent the varactor diode from becoming forward biased and stopping the oscillator.

Strobe Driver Circuit

The Strobe Driver circuit consists of ÷ 5 counter U1022, bandpass filter FL2064, source follower Q2091, and AND gate U1091A and U1091B.

The Controlled Oscillator signal is applied to the clock input of counter U1022 which is wired to divide the input signal by five. The STROBE ENABLE 1 line from the Error Amplifier permits the counter to operate when the line is low

and is the means by which the microcomputer can shut off or turn on the strobe pulses. The output of the counter, which ranges from 5.006 MHz to 5.019 MHz, is coupled through an impedance matching network consisting of C2030, L1031, C2033, and C1032. This circuit raises the line impedance to about 8200 Ω. The signal is then passed through monolithic bandpass filter FL2064, through another impedance matching network, to the gate of Q2091. The signal is coupled from the source of Q2091 to the inputs of U1091A and U1091B, both of which are configured as buffers. U1091B drives the Phase Gate circuitry, and U1091A is reserved for future applications. Capacitors C1032 and C2105 are selected to provide maximum signal amplitude at TP2087.

DIGITAL CONTROL ⟨9⟩

The Digital Control section of the 492/492P provides the operator/492 and digital controller/492 interfaces. It translates changes in front-panel controls and instructions received via the accessories interface or GPIB interface (492P only) into codes that control the instrument via the instrument bus.

The Digital Control section simplifies operating and programming the 492 and 492P. Unless overridden by the operator, the microcomputer automatically selects secondary parameters. Some examples are: when the operator selects span, the microcomputer chooses an appropriate bandwidth; when the operator changes the reference level, the microcomputer trades off input attenuation and IF gain.

In the 492P, the microcomputer can handle some operations automatically. Some examples are: the microcomputer can set PEAKING for best response; the microcomputer can search digital storage for signals and change FREQUENCY and REFERENCE LEVEL to zoom in on signals it finds.

The digital control operating program is defined by the meaning of the controls and commands given in the operating and programming manuals and is not further defined here. The following description focuses on the hardware.

The following circuits make up the digital control section:

1) microcomputer, including processor and memory boards;

2) addressable registers on the instrument bus;

3) front panel Accessories interface;

4) GPIB interface (492P only).

The microcomputer is based on a 6800 microprocessor; its operating program is stored in ROM. The microprocessor accesses the ROM-RAM, and I/O interface via the microcomputer bus. The bus operates with 16-bit addresses, 8-bit bytes, and several control lines for data transfers.

The front panel and the addressable registers that control some other 492/492P assemblies reside on the instrument bus. This bus requires only 8-bit addresses and transfers 8-bit bytes. The bytes may be codes to set or indicate the status of an assembly or, in the case of digital storage and crt readout, data values that correspond to the display. When one of the assemblies requires the attention of the microcomputer, it asserts a service request line. The microcomputer responds by finding the source of the service request and executing the appropriate service routine.

Processor communication over the instrument bus can be stopped by an external controller on the accessories bus; the external controller can then override normal operation.

The GPIB interface (492P only) resides on the microcomputer bus. It contains added ROM for the operating program used for GPIB I/O and added RAM. The interface is based on a general-purpose interface adapter (GPIA) IC that reduces processor overhead required for GPIB operation.

PROCESSOR ⟨31⟩

The Processor board contains the processor clock, microprocessor, address decoders, microcomputer bus buffers, and instrument bus interface. These blocks are shown on the Processor board block diagram adjacent to Diagram 31.

Processor Clock

The two-phase processor clock is derived by U4035 from its internal oscillator. A simple logic diagram of this IC is shown in Fig. 5-30.

The two clock signals, $\phi1$ and $\phi2$, are complementary and non-overlapping. They are divided by 4 from the oscillator frequency for a processor clock frequency of about 850 kHz. The $\phi2$ CLK is buffered for use by the rest of the microcomputer system and is in phase with the $\phi2$ clock signal used by the 6800. The undivided oscillator frequency signal is distributed as CRT CLK for crt readout timing.

RST stays low while C3042 charges following power-up and holds the microcomputer in a reset state until the power supply is fully on. This signal does not disable the clock, so the 6800 can initialize itself during this time.

6800 Microprocessor

The 6800 microprocessor (U3027) is an 8-bit processor with an 8-bit bidirectional data bus and 16-bit address bus. The 6800 block diagram in Fig. 5-31 shows the internal organization of the IC. The function of each block is as follows.

Accumulators. Eight-bit accumulators A and B hold operands for and results of ALU operations.

Condition Code Register. Bits in the condition code register indicate results of ALU operations and whether interrupts are masked; see Table 5-20.

Program Counter. This 16-bit register holds the address of the instruction being executed.

Stack Pointer. This 16-bit register acts as the pointer for a previously defined stack in memory. The pointer is the address of the next available location on a LIFO (last-in, first-out) basis. The stack is used to store the contents of MPU registers when an interrupt occurs or the 6800 executes a subroutine. The stack pointer is decremented when data is pushed onto the stack and incremented when data is popped off the stack.

Table 5-20
CONDITION CODES

0	Carry from accumulator bit 7
1	Overflow
2	Zero result
3	Negative result
4	Interrupt mask
5	Carry from accumulator bit 3 (half-carry)
6	Unused (always 1)
7	Unused (always 1)

Index Register. This 16-bit register facilitates indexed-mode addressing. Instructions can load, increment, decrement, compare, etc., so it can also be used as a general purpose register.
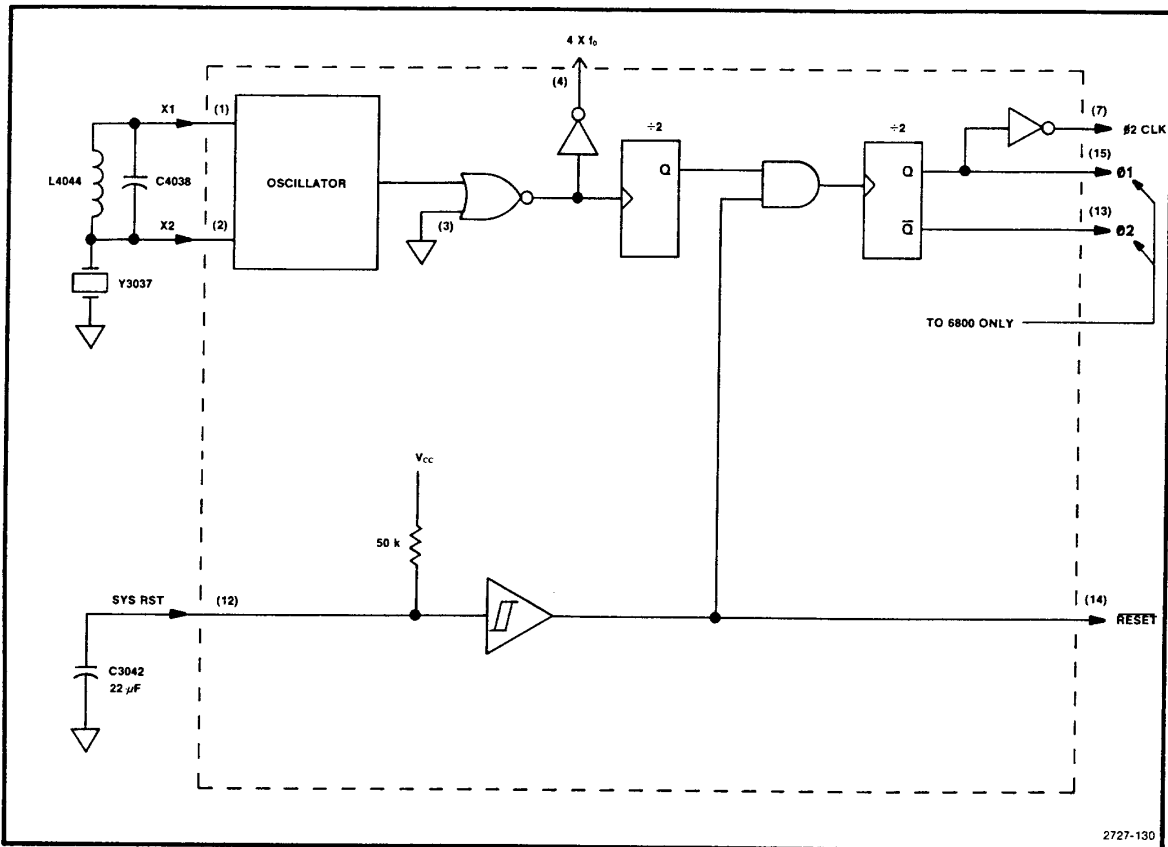
Fig. 5-30. Simple logic diagram of processor clock.

Instruction Register and Decoder/Timing Control. During the instruction fetch (the first one or more machine cycles), successive bytes of an instruction are loaded from the program memory into the instruction register. The contents of this register are then passed to the decoder and timing logic. This block decodes the byte(s) and generates the machine states and control signals that affect execution of the instruction. The number of machine cycles this takes depends on the instruction and addressing mode.

Data and Address Buffers. These tri-state buffers isolate the 6800 internal buses from the external microcomputer bus.

Clocks. The two-phase TTL-level clock signals synchronize 6800 operation. A machine cycle is defined as the interval between two successive positive-going transitions of the $\phi 1$ clock signal.

$\overline{\text{HALT}}$. This input is unused (tied high through a pull-up).

Three-State Control (TSC). This input is tied low so the address buffer and read/write line are always enabled.

Read/Write (R/$\overline{\text{W}}$). This output sets the direction of data flow—high when the 6800 is reading data and low when the 6800 is writing data. It is also high between read and write operations.

Valid Memory Address (VMA). This output is asserted high when the 6800 places a valid address on the microcomputer bus. It enables the memory address decoders.

Data Bus Enable (DBE). This input is paired with the $\phi 2$ clock input so the data buffer is enabled during $\phi 2$ of the machine cycle.

Figure 5-32 shows a read and a write cycle on the microcomputer bus. This illustrates how the control signals are used to control data transfers on the bus.
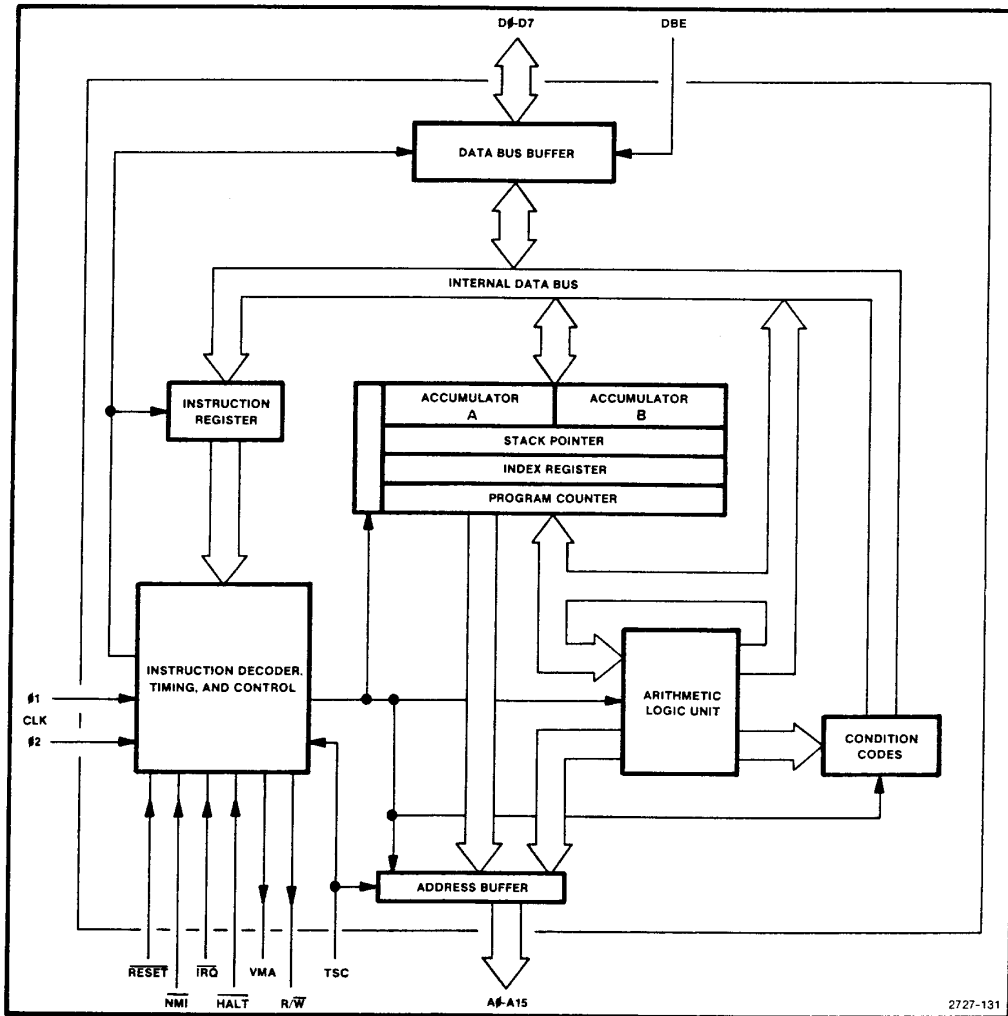
Fig. 5-31. Block diagram of 6800 microprocessor.

Interrupt Request (IRQ). This input is buffered from SER REQ on the instrument bus. When one of the assemblies asserts this line, it is seeking the microcomputer's attention. The 6800 completes its current instruction before reacting. It then checks the interrupt mask bit in the condition code register. This bit is set when the microcomputer is executing most service routines in response to front-panel changes or GPIB messages. If the bit is set, the request is ignored until the microcomputer completes the routine and resets the bit. If the bit is clear, the microcomputer sets the bit and then starts an interrupt sequence.

1. Push the contents of the program counter, index register, accumulators, and condition code register onto the stack, decrementing the stack pointer each time a byte is stored.

2. Set the interrupt mask bit and load the address stored at FFF8, the interrupt vector.

NOTE

6800 addresses are given as hexadecimal numbers.

3. Execute the interrupt service routine that begins at the address read in step 2. This routine begins by interrogating the assemblies to find one that pulled down on the interrupt request line. It then proceeds to service that assembly.

4. At the end of the interrupt routine, return to the idle routine that occupies the microcomputer between tasks by retrieving the previous register contents from the stack.
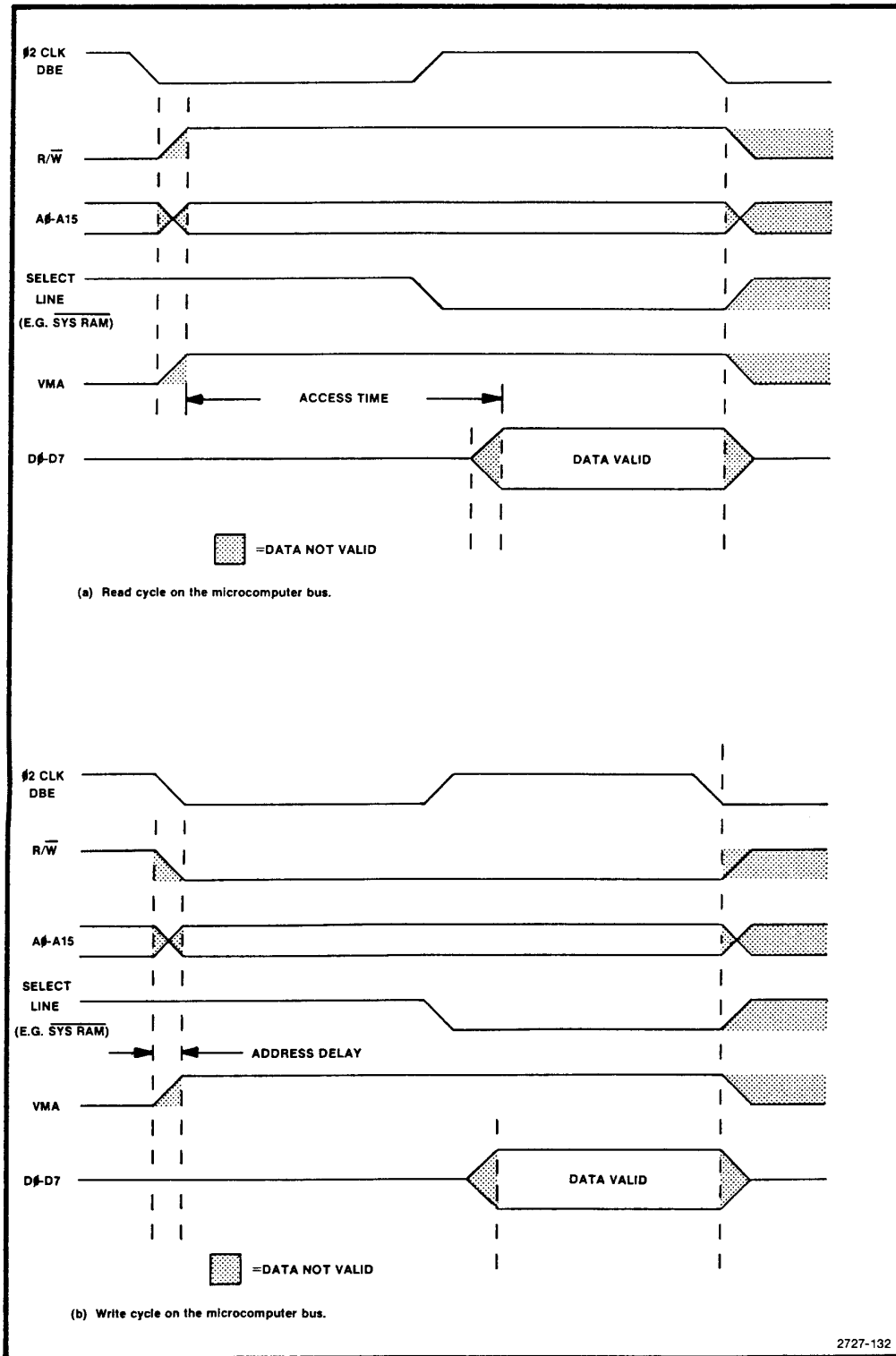
Fig. 5-32. Read and write cycle timing on the microcomputer bus.

Non-Maskable Interrupt (NMI). Tied high through a pull-up, this interrupt is not used by the digital control system.

RESET. This input initializes the 6800 following power-up. The clock generator (U4035) holds this line low for about one second for 6800 start-up. After the input goes high, the 6800 begins its initialization routine at the address stored at FFFE and FFFF. This routine masks interrupts until it is ready to handle them. It then continues executing the operating program according to the flow chart in Fig. 5-33.

6800 Address and Data Bus

The 6800 address outputs are buffered by U2035 and U3036; they are always enabled. The data I/O buffer, U1013, is normally enabled. If disabled by P1020, it isolates the 6800 from the microcomputer bus data lines for diagnostics. See further information about diagnostics under Address Decoders. The direction of data flow is set by the R/W line.

Address Decoders U2044 and U1037B drive address select lines and status lights for the microcomputer system. The address select lines are shown in Table 5-21.
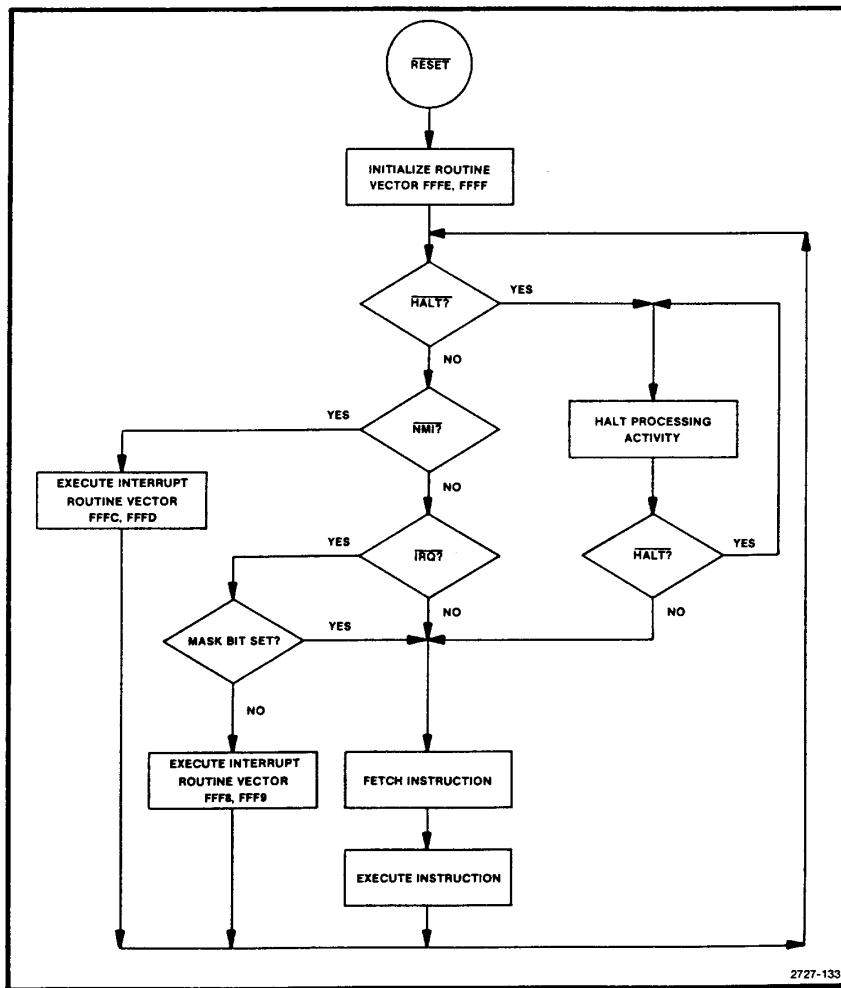
Fig. 5-33. Flow chart of the 6800 main decision paths.

Table 5-21
ADDRESS SELECT LINES

Line	Selects	Address
SYS RAM	RAM on Memory board	0000—07FF
GPIB RAM	RAM on GPIB board	0800—OFFF
U1037B-12	Instrument bus	1000—11FF
GPIB	GPIA on GPIB board	1200—13FF
OPSW	Switch register on Memory board	1400—15FF

Table 5-22
492/492P MICROCOMPUTER ADDRESS SPACE

0000

            System RAM
0800

            GPIB RAM
1000

       Instrument Bus Interface
1200

       GPIA on GPIB board
I/O
1400

      Options switch on Memory board
1600

            Unused
1800

  ROM on Memory board (Four 2K EPROM's)
3800

            Unused
4000

  ROM on GPIB board (B 2K EPROM's or 2
          8K ROM's)
8000

  ROM on Memory board (Four 8K sockets
   with 2K EPROM's or 8K ROM's)
FFFF

Other addresses are decoded on the Processor board for diagnostics, turning on LEDs on some outputs of U2044. Diagnostic routines can cause the 6800 to access an address that turns on an LED as a test indicator. For further information, see the self-test instructions in the Maintenance section.

ROM addresses on the Memory board and the GPIB board are decoded there and do not rely on address select lines from the Processor board.

U2044 is enabled by VMA and zeros on A15 and A14 (3FFF and below). It decodes the 3-bit binary input of A11, A12, and A13 to assert one of eight outputs (Y6 and Y7 are unused).

U1037B is enabled when U2044 decodes an address in the range 1000—17FF and decodes A9 and A10 to assert one of four outputs.

Address Map

Microcomputer memory is mapped in Table 5-22 (addresses in hexadecimal).

Instrument Bus Interface

The microcomputer communicates with the rest of the instrument over the instrument bus (with the notable exception of the GPIB interface). Peripheral interface adapter (PIA) U3022 is programmed to send addresses and send or receive data on the instrument bus. It also handles control lines for writing to and reading from registers on the instrument bus. It does not, however, handle service requests; the SER REQ line goes directly to the 6800.

The PIA is reset at power-up and the 6800 then programs it for each of its tasks. How the 6821 PIA is configured in the 492/492P microcomputer system is shown in Fig. 5-34.

Chip Select. Chip select lines CS0 and CS1 are always enabled; the 6800 selects the PIA by addressing 1000,
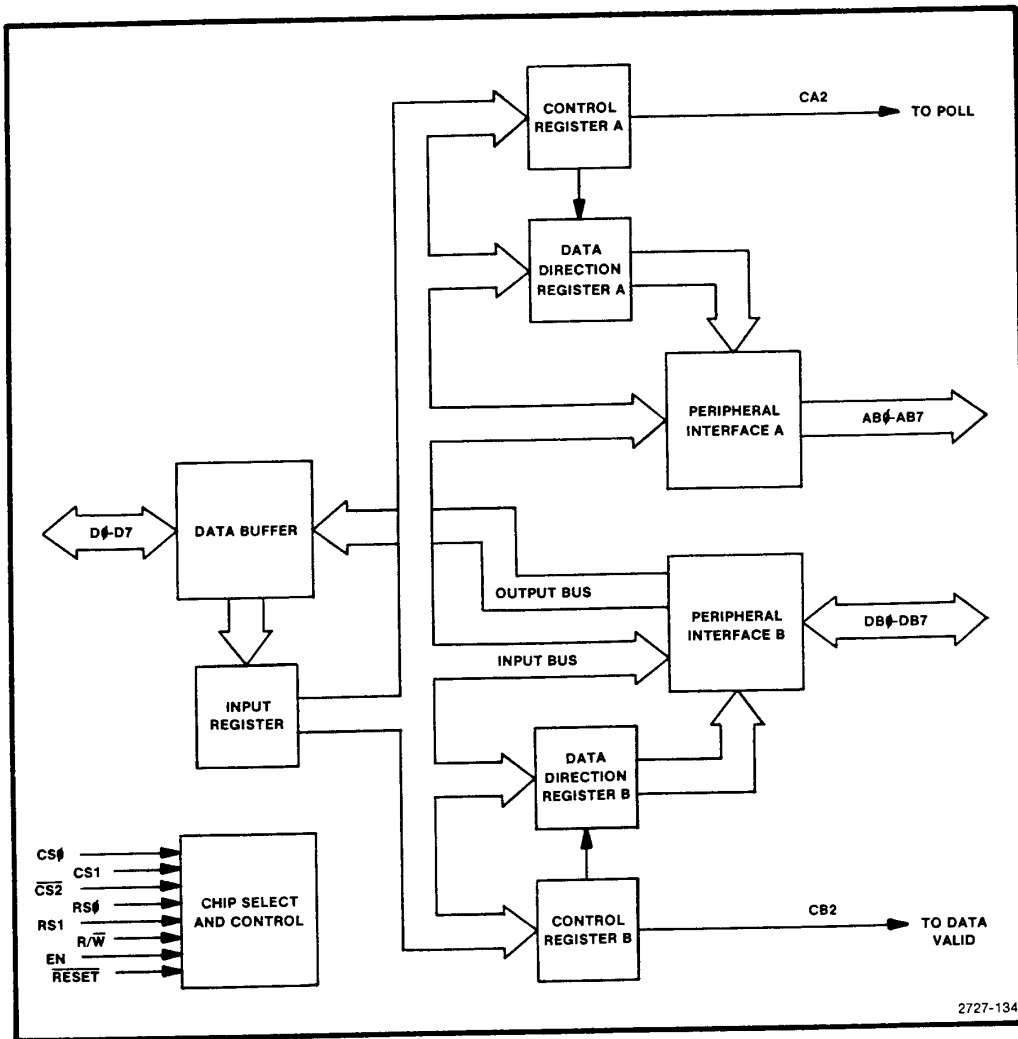
Fig. 5-34. 6821 PIA registers and control lines.

which asserts CS2. Data transfers are then performed under control of the read/write, register select, and enable signals.

Register Select. Four registers and two peripheral interfaces are addressable. The 6800 selects one by a code on RS0 and RS1 (the two LSBs of the PIA address) and by setting or clearing bit 2 in the appropriate control register as shown in Table 5-23.

Read/Write. The 6800 sets the direction of data through the data buffer with R/W̄. When the 6800 sets this line low, it enables the input register. A high enables input to the 6800 from the PIA internal output bus.

Enable. The $\phi2$ clock high pulse transfers data to the input register and enables one of the peripheral interfaces (if addressed) on a write cycle.

Data Direction Registers. These registers allow the MPU to control the direction of data on each line connected to the peripheral interfaces. A zero (0) configures the corresponding data line as an input; a one (1) configures it as an output.

Control Registers. The 6800 uses bit 2 of these registers for addressing as explained above. Bits 3, 4, and 5 form a code to control CA2 and CB2 as outputs on the instrument bus. CA2 is configured as POLL to enable a parallel poll on the instrument bus. CB2 is configured as DATA

REV AUG 1981

VALID to strobe data into an addressed register during a 6800 write to the instrument bus. It is also asserted on 6800 reads to enable the data buffer. The RC delay following inverter U1013B provides data settling time on the bus before DATA VALID goes high. U1013B's open-collector output pulls down faster than R1024 pulls up, so DATA VALID's low-high transition is delayed compared to its high-low transition.

Peripheral Interface A. PA0—PA7 are configured as outputs to drive the instrument bus address lines. The 6800 writes to this interface to address a register on the instrument bus.

Both the A and B interface buffers are disabled if an external controller pulls the INTL CONT line low. They are also disabled if P1020 is disconnected for diagnostic purposes. Either releases the low on the output of U1037A. The interrupt line buffer, U3043A, is also disabled. These buffers for the address, data, and interrupt lines then decouple the 6800 from the instrument bus.

The MSB of the address determines the direction of data through U3016, the data lines buffer. Instrument bus addresses 80 and above set U3016 to buffer data from the instrument bus to the PIA (6800 read); address 7F and below set U3016 to buffer data in the opposite direction (6800 write).

Peripheral Interface B. PB0—PB7 are configured either as inputs or outputs to transfer data from or to the instrument bus. The 6800 writes data to this interface to send it to a register on the instrument bus and reads data from this interface when it interrogates a register on the instrument bus.

Pull-ups on the data lines result in all ones if a read cycle inputs a byte when no instrument bus register is enabled.

The RC delay in the enable signal for buffer U3016 slows the low-high transition at the input of the Schmitt trigger, but has little effect on the high-low transition. This holds the instrument bus data lines stable while DATA VALID is going false, but has little effect when the data lines are to be driven at the beginning of a write cycle.

Instrument Bus Registers

Instrument bus address lines are split into a right bus and a left bus for economy in address decoding. On the right bus, a board with an addressable register need only decode AB0 through AB3 and AB7; on the left bus, a board need only decode AB4 through AB7. In both cases, AB7 indicates read (high) or write (low), as it does for the instrument bus interface data buffer noted above. The microcomputer communicates with the following registers to control assemblies as shown in Table 5-24.

Instrument Bus Data Transfers

Data transfers on the instrument bus require two steps: the 6800 writes the address to peripheral interface A and then reads or writes the data through peripheral interface B.

When the 6800 writes to the instrument bus, it configures the PIA to pulse DATA VALID (the CB2 output). The PIA does this automatically after data is written to peripheral interface B as shown in Fig. 5-35.

Table 5-23
PIA REGISTER AND INTERFACE SELECT CODES

		Control Register Bit		
RS1	**RS0**	**CRA-2**	**CRB-2**	**Register or Interface**
0	0	1	X	Peripheral Interface A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Interface B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

Table 5-24
INSTRUMENT BUS REGISTER ADDRESSES

---------- Right Bus ----------

Register	Circuit Board	Write	Read
Tune control data	Center Frequency Control	70	F0
Data steering	Center Frequency Control	71	
1st LO driver control	1st LO Driver	72	
1st LO phaselock control	Phaselock Control	73	F3
Front panel LEDs	Front Panel	74	
Front panel encoders	Front Panel		F4
Span magnitude data	Span Attenuator	75	
Span magnitude and decade attenuator data	Span Attenuator	76	
Control data	Preselector Driver	77	
Option configuration	Preselector Driver		F7
Post VR gain	Log & Video Amplifier	78	
Video display mode/gain	Log & Video Amplifier	79	
Digital storage data	Vertical Digital Storage	7A	FA
Digital storage control	Vertical Digital Storage	7B	
Video level/filter/blank	Video Processor	7C	

---------- Left Bus ----------

Sweep rate and mode	Sweep	0F	
Holdoff, interrupt, trigger	Sweep	1F	
Crt readout data	Crt Readout	2F	
10 MHz IF gain and bw	VR Motherboard #2	3F	
Z-axis & RF deck control	Z-Axis/RF Interface	4F	
Crt readout control	Crt Readout	5F	

When the 6800 reads from the instrument bus, it does not configure the PIA to pulse DATA VALID as it does for a write cycle. Rather the 6800 writes to control register B to set CB2 low. CB2 low asserts DATA VALID, after the RC delay allowing for the data to be accessed, and the 6800 then reads the data through peripheral interface B. After reading the data, the 6800 writes again to control register B to unassert DATA VALID.

Instrument Bus Poll

When the 6800 recognizes an interrupt request (SER REQ asserted), it enters a service routine. As part of this routine, it performs a parallel poll to find who is requesting service. A parallel poll sequence is shown in Fig. 5-36.

The 6800 begins by writing an invalid address on the instrument bus, FF; all address decoders on the bus ignore this address. Next, the 6800 writes to control register A to set CA2 high, asserting POLL. All boards that respond to a poll recognize this line and contain logic that either responds or prepares to respond when the 6800 causes DATA VALID to be asserted. Each interrupt is assigned a data line as shown in Table 5-25. The board originating that interrupt pulls low on the corrsponding line.
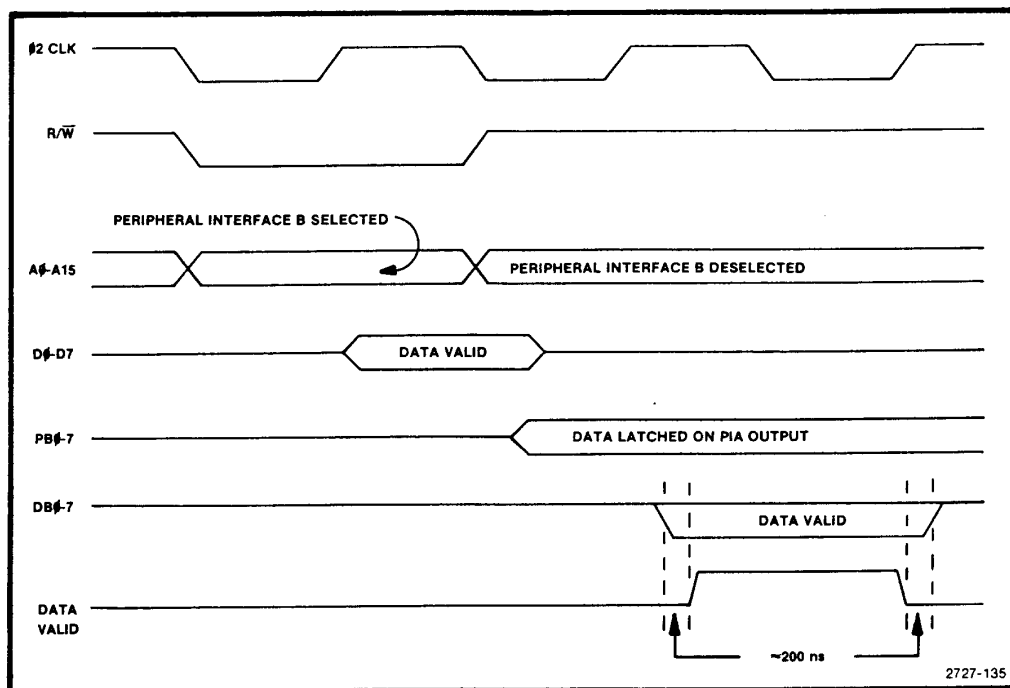
Fig. 5-35. A 6800 write to the instrument bus.

Table 5-25
PARALLEL POLL BYTE

7	6	5	4	3	2	1	0
X	X	X	End-of sweep	Center frequency knob	Phase lock	X	Front panel encoder

After the 6800 reads the status byte, it clears POLL and writes address 7F on the instrument bus. The transition on POLL disables the poll response circuitry of boards on the instrument bus. Since 7F is also an invalid address, it also unaddresses all instrument bus registers. The following positive transition on POLL prepares all parallel poll boards, so when the 6800 writes back the parallel poll byte, it clears all interrupts that were read.

The 6800 reads the interrupt status of the GPIA on the GPIB board separately and combines it with the instrument bus status before servicing the interrupt(s). Interrupts are serviced according to their priority.

MEMORY BOARD ◇32◇

The Memory board holds the ROM operating program for the microcomputer and the RAM used by the program. It also holds a bank of switches that the microcomputer can read to configure itself for options and diagnostics.

ROM Address Decoding

The full microcomputer address bus extends to this board for ROM address decoding. U1036 and U1038 decode banks of addresses and assert one-of-eight ROM chip-enable lines when a bank that corresponds to one of the ROMs is addressed. The decoders are enabled by VMA and R/W high (a valid address during a read cycle). U1036 also requires A15 to be low to be enabled; if enabled, it decodes addresses in the range 1800 to 3800 from the binary code formed by A11 through A13.

Since U1038 alone responds to the upper-half of address space, it need not decode addresses further than A13 through A15. The four ROMs in this address space, howev-
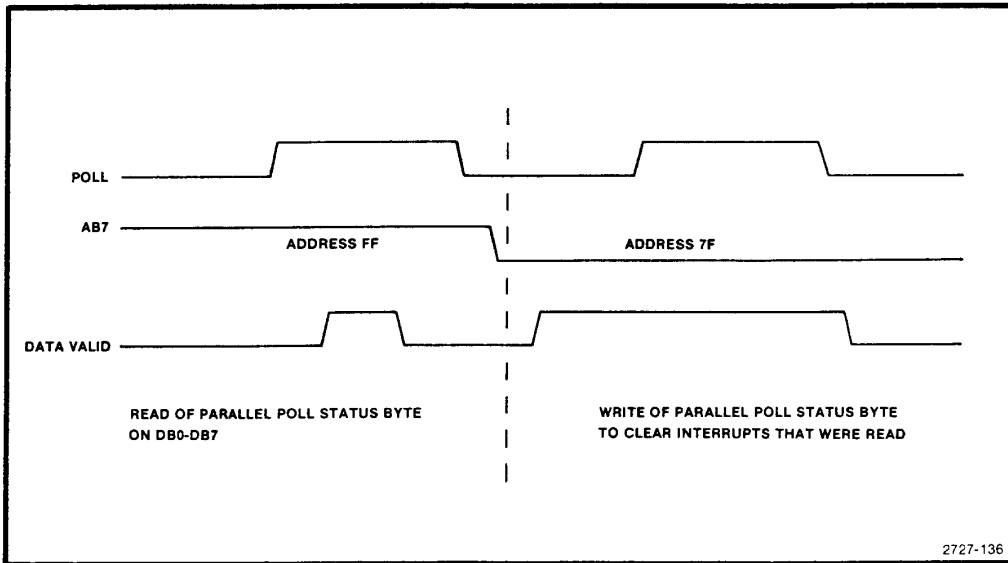
Fig. 5-36. Instrument bus poll sequence.

er, are strapped to treat the enable and the upper address bits differently if 8k rather than 2k chips are installed. For 8k, the decoded enable lines drive the chip-enable inputs and the upper address bits (A12 and A11) are decoded by the chip. For 2k, the decoded enable line, rather than A11, drives pin 18, and a logic one, rather than A12, is applied to pin 21; pin 20 is grounded. The decoder responds to $\phi2$ CLK so the enable lines are clocked for the benefit of 8k ROMs, which recognize a new address only on the negative transition of $\overline{CE}$.

RAM

Data words in RAM are divided between the two 1k X 4 ICs; U2032 holds the upper four bits and U2035 holds the lower four bits. Both are selected by SYS $\overline{RAM}$ and the $\phi2$ clock, while R/$\overline{W}$ sets the data direction.

Option Switch Register

The microcomputer accesses U1033, a buffer enabled by $\overline{OPSW}$, to read S1033 at power-up. Switch 1 indicates Option 08 (open) or non-option 08 (closed). Switches 2 through 6 indicate internal hardware configuration. Switches 7 and 8 call self-test routines. For the correct use of switches 2 through 8, refer to the Maintenance section of this Service manual.

FRONT PANEL ◇30◇

The Front Panel board translates an operator action of a front-panel control into data for the microcomputer to read

and implement. The board, in turn, accepts data from the microcomputer to display via LEDs of the current operating modes of the instrument. Some analog control signals are also derived from potentiometers on this board.

Push button switches and some rotary switches are wired in a matrix that is read by a keyboard encoder; this is the main switch encoding block. A power-up circuit prompts the encoder to output the initial value of the rotary switches. The FREQUENCY control drives a separate up/down encoder. Each encoder interrupts the microcomputer when it senses a change and transmits its data through the instrument bus port.

The LED display inputs data through the instrument bus port and strobes it into shift registers that drive the LEDs.

Instrument Bus Port

The instrument bus port comprises an address decoder, an output path for the encoders, and an input path to the bank of LED driver shift registers. The output and input paths appear as registers on the instrument bus.

Address Decoding. The data and enable inputs to U4031 select output Y2 when the microcomputer places address 74 on the instrument bus and output Y6 for address F4. These addresses correspond to the input and output paths through the port:

Hex address   Data path

74   Input to LED display shift registers and pow-er-up circuit.

F4   Output from keyboard and frequency encoders.

Input. DB0, DB1, DB2, and DB4 provide the inputs to shift registers U2045, U3030, U5045, and U6075. The microcomputer writes to this input port eight times to fill the shift registers, which drive the front-panel LEDs. The MSB of U6075 drives the graticule light circuit.

DB3 drives the power-up circuit.

Output. DB0 through DB6 represent the 7-bit code from the keyboard encoder. The code corresponds to one of the positions shown in Fig. 5-39 under Switch Matrix Codes. The X-Y positions of the switch can be decoded from the 7-bit code as a decimal number in which the first digit is X and the rest of the number is Y. To obtain the number:

1) convert the binary code to decimal number;

2) add 1 to the first digit and 1 to the second digit;

For example:

1) binary 0011101 is converted to decimal 29;

2) 1 is added to the first digit (2), and 1 is added to the second digit (9), for $X=3$ and $Y=10$—the FINE button.

DB7 represents the direction of change in the FRE-QUENCY control (see FREQUENCY Encoder that follows).

Buffer U1047 is enabled only when the output path is addressed.

Switch Encoding

A keyboard encoder, U3039, scans the switch matrix continuously and compares any switch closures it senses with those sensed during the last scan. Any new closure causes the encoder to request service so the microcomputer can read the code for the switch.

How the encoder scans the matrix is illustrated in Fig. 5-37. By asserting X1 through X8 in turn, the encoder ac-cesses a column of switches. It senses the state of each switch in that column on Y1 through Y10.
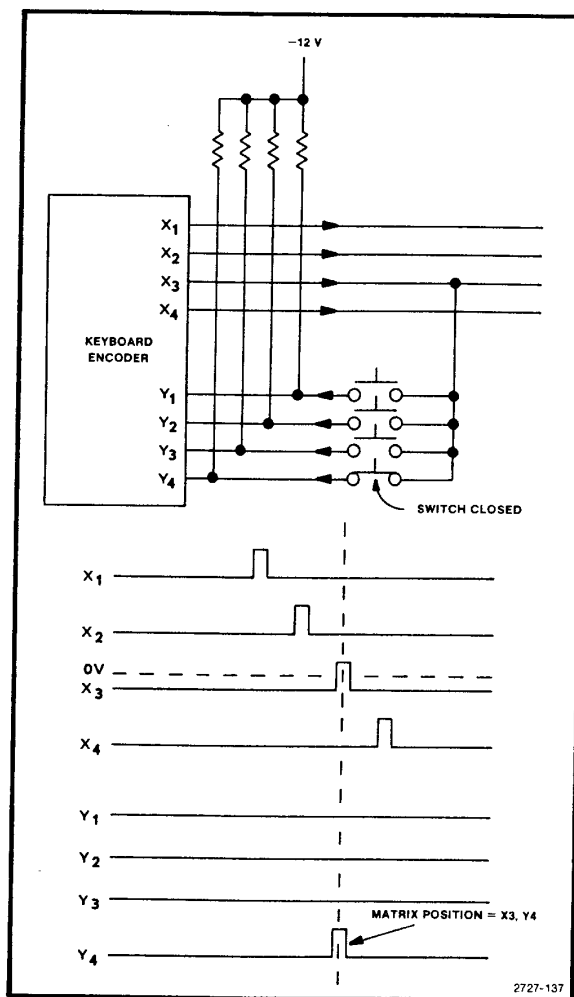
Fig. 5-37. Scan by simplified keyboard encoder.

Encoder Logic. The logic inside the keyboard encoder that scans the matrix, senses switch closures, handles the bookkeeping for which switches changed, and outputs the code for new closures, as shown in Fig. 5-38.

The keyboard encoder is clocked by a 555 timer, U1011. The clock drives the Y counter, which causes the key sense logic to present the status of each of its inputs, Y1 through Y10, sequentially to the control logic. These inputs repre-sent the state of a column of switches in the switch matrix. The control logic continuously shifts through the shift regis-ter to compare the input from the key sense logic to the value last stored for the switch represented by that input. When a scan of the column is finished, the X counter ad-vances so the next column is scanned.
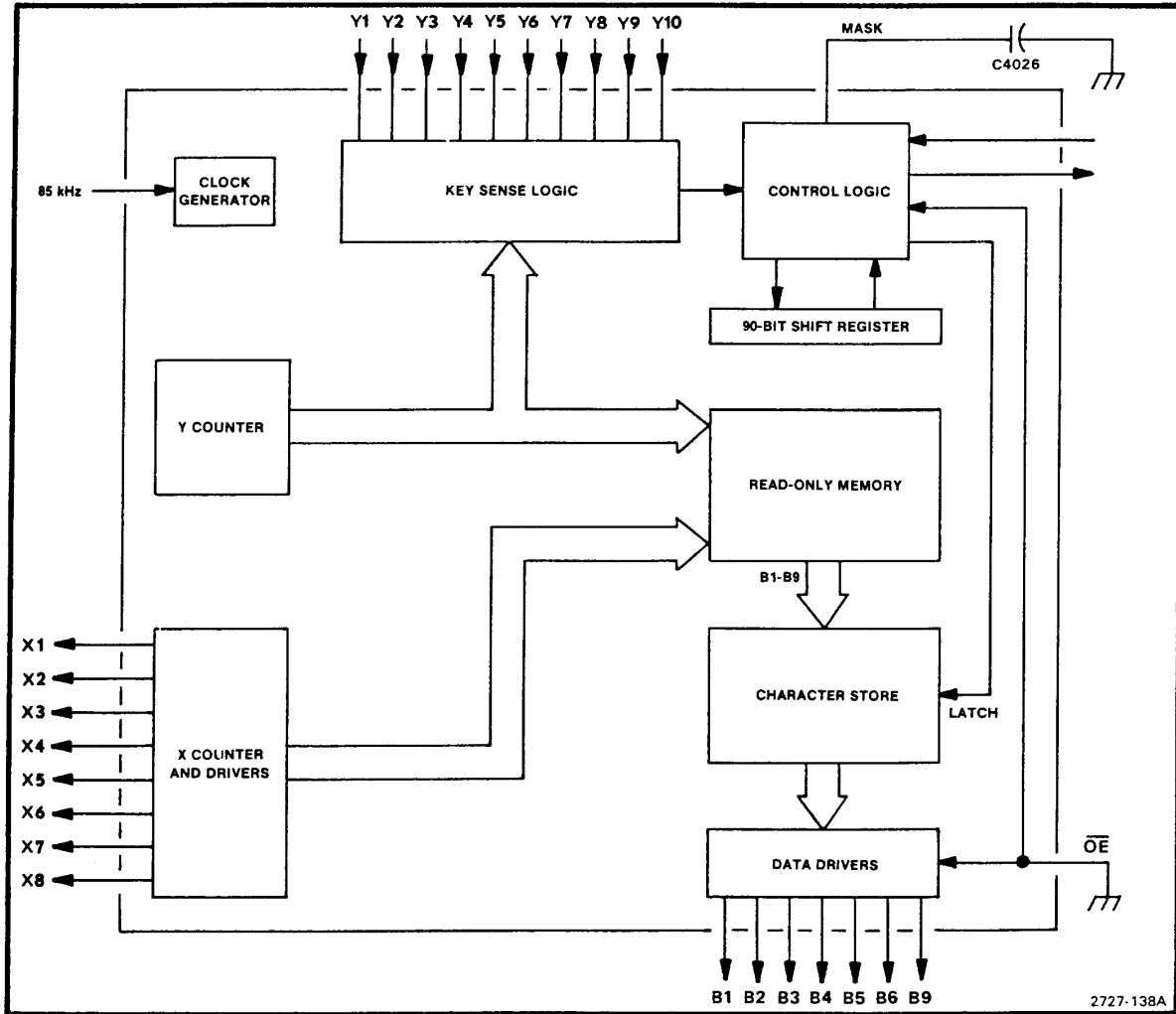
Fig. 5-38. The keyboard encoder.

When the control logic detects a difference between the input and a bit in the shift register, it activates the debounce mask, its latch output, and the encoder strobe output. The mask signal holds off action by the control logic so the encoder doesn't see multiple switch closures caused by switch bounce. The mask time is controlled by C4026. The latch output causes the character code, in read-only memory, addressed by the X and Y counters, to be entered in the character store. The encoder strobe output activates the encoder interrupt interface to request the microcomputer's attention.

Switch Interrupt Interface

The encoder strobe output is level controlled by the switch interrupt interface. When the encoder asserts its strobe output (high), it causes U3014C to pull down on $\overline{SER}$ $\overline{REQ}$. The strobe high also releases the preset input to U2018B, which was holding the keyboard encoder strobe control input low. Since the encoder is waiting for a low-to-high transition on this input, to stop asserting its strobe output, $\overline{SER\ REQ}$ remains asserted.

When the microcomputer responds to the interrupt, it learns that the keyboard encoder requested service from DB0, the encoder's parallel poll bit. DB0 is set low by U3014E at the same time $\overline{SER\ REQ}$ is asserted. The microcomputer ends its poll sequence by clearing all interrupts it has read. It does this by first setting AB7 low, disabling U3014E so it cannot continue to assert DB0. The microcomputer then writes the parallel poll byte back on the

instrument bus. If the encoder was requesting service, the low on DB0, when written back, is clocked into U2018B when POLL is removed by the microcomputer. The output of U2018B then cancels the encoder strobe with its low-to-high transition.

Switch Matrix. The switch matrix includes both momentary contact and rotary switches. One side of each switch is connected to −12 V through a resistor in parallel with a Y input. The other side of the switch is connected in parallel with the other switches in the column to an X output.

When an X output is asserted, the Y inputs remain at a negative voltage unless a contact is closed. If the contact is closed, the X output raises the Y input for that switch to a positive voltage. Rotary switches occupy as many positions in the matrix as they have contacts. The switches are wired to yield the codes shown in Fig. 5-39.

Rotary switches for RESOLUTION BANDWIDTH and SPAN/DIV are a special case. Although each occupies four positions in the matrix, the two are used only as up/down prompts to the microcomputer to change the corresponding parameter. The microcomputer notes the initial setting and changes the parameter accordingly when the switch is moved, keeping track of the direction the switch was changed by comparing its new position to its old.

Power-up Circuit. When the microcomputer performs its power-up routine, it writes a 1 in bit 3 address 74. Because this bit is not latched, the microcomputer continues to write this 1 in the bit while the keyboard encoder is initialized.

The keyboard encoder is initialized by setting to zero the bits in the shift register that represent the rotary switches.

This happens because:

1) writing a 1 to bit 3 sets both inputs of U3012A high, turning off Q6028;

2) Q6028 off allows −12 V to be applied through R6028 to the rotary switch X inputs. This overrides the keyboard encoder X scan signals, so the Y inputs remain low without regard to the position of the switch;

3) because the microcomputer continues to write a 1 in bit 3, the keyboard encoder is given enough time to update its shift register with all zeros representing the rotary switch contacts.

After the keyboard encoder is initialized, the microcomputer resets bit 3. This restores the switch matrix to normal operation, and the keyboard encoder reads the position of the rotary switches as changes in the switch matrix. It outputs these apparent changes to the microcomputer, which interprets them as the power-up values for TIME/DIV and MINIMUM RF ATTENUATION and the initial switch position for REFERENCE LEVEL, FREQUENCY SPAN, and RESOLUTION BANDWIDTH.

FREQUENCY Encoder

The center frequency control is a rotary switch that generates a gray code. It is decoded as shown in Fig. 5-40.

Up/Down Encoding. The gray code changes one bit at a time, causing U6025A to change state for each position change of the switch. This pulses a low on the input of either U5025B or U5025C (the other input remains high), making the inputs to U6025B momentarily unequal. As a result, U6025B pulses the set input of U4015B to assert $\overline{SER}$ $\overline{REQ}$.

The same pulse is inverted to clock the up/down flip-flop, U4015A. This flip-flop records the direction of change in the switch, determined by the exclusive-OR of the previous state of B and the current state of A. The trailing edge of the pulse from U6025B updates U2018A to remember the current state of B for the next cycle.

Exclusive-OR U6025D detects the direction of change in the FREQUENCY control because of the property of the gray code. Down (counterclockwise) yields unequal inputs when the previous state of B is compared to the current state of A, while up (clockwise) yields the opposite. The up/down condition is clocked into U4015A and is read by the microcomputer as the MSB of the output port.

FREQUENCY Interrupt Interface

In its quiescent stage, U4015B is held cleared by the feedback from its Q output to its clear input. A low on its set input temporarily forces U4015B to set both its outputs high, allowing the low on the set input to set the flip-flop. When set, U4015B asserts $\overline{SER}$ $\overline{REQ}$ and drives U3014F to assert DB3 when the microcomputer performs a poll. U3014F is enabled during a poll as noted above for interrupts under Switch Encoding. U4015B is cleared (if it was asserting DB3) when the microcomputer writes back the parallel poll byte to clear all interrupts that were read.

Potentiometers

Some controls generate analog signals used by other functions in the instrument. These controls are non-programmable.

TIME/DIV · MIN RF ATTEN

	X1	X2	X3	X4	X5	X6	X7	X8
Y1	20 µs 00	50 ms 0A	EXT TRIG 14	INT TRIG 1E	READOUT 28	0dB 32	SPAN DIV 3C	REF LEVEL 46
Y2	50 µs 01	.1 s 0B	SINGLE SWEEP 15	FREE FUN 1F	GRAT ILLUM 29	10 dB 33	3D	47
Y3	.1 ms 02	.2 s 0C	B-SAVE A 16	SAVE A 20	FUTURE USE 2A	20 dB 34	3E	48
Y4	.2 ms 03	.5 s 0D	2 dB/ DIV 17	LIN 21	MAX HOLD 2B	30 dB 35	3F	49
Y5	.5 ms 04	1 s 0E	VIEW B 18	NARROW FILTER 22	BASE-LINE CLIP 2C	40 dB 36	40	
Y6	1 ms 05	2 s 0F	10 dB/ DIV 19	WIDE FILTER 23	ΔF 2D	50 dB 37	RESOLUTION BW 41	
Y7	2 ms 06	5 s 10	DEGAUSS 1A	VIEW A 24	CAL 2E	60 dB 38	42	
Y8	5 ms 07	AUTO 11	MIN NOISE 1B	PHASE LOCK 25	AUTO RES 2F		43	
Y9	10 ms 08	MNL 12	FREQ RANGE 1C	FREQ RANGE 26	PULSE STETCH-ER 30		RESET TO LOCAL 44	
Y10	20 ms 09	EXT 13	FINE 1D	IDENTIFY 27	EXT MIXER 31		LINE TRIG 45	

SWITCH NAME OR POSITION

LIN — 21

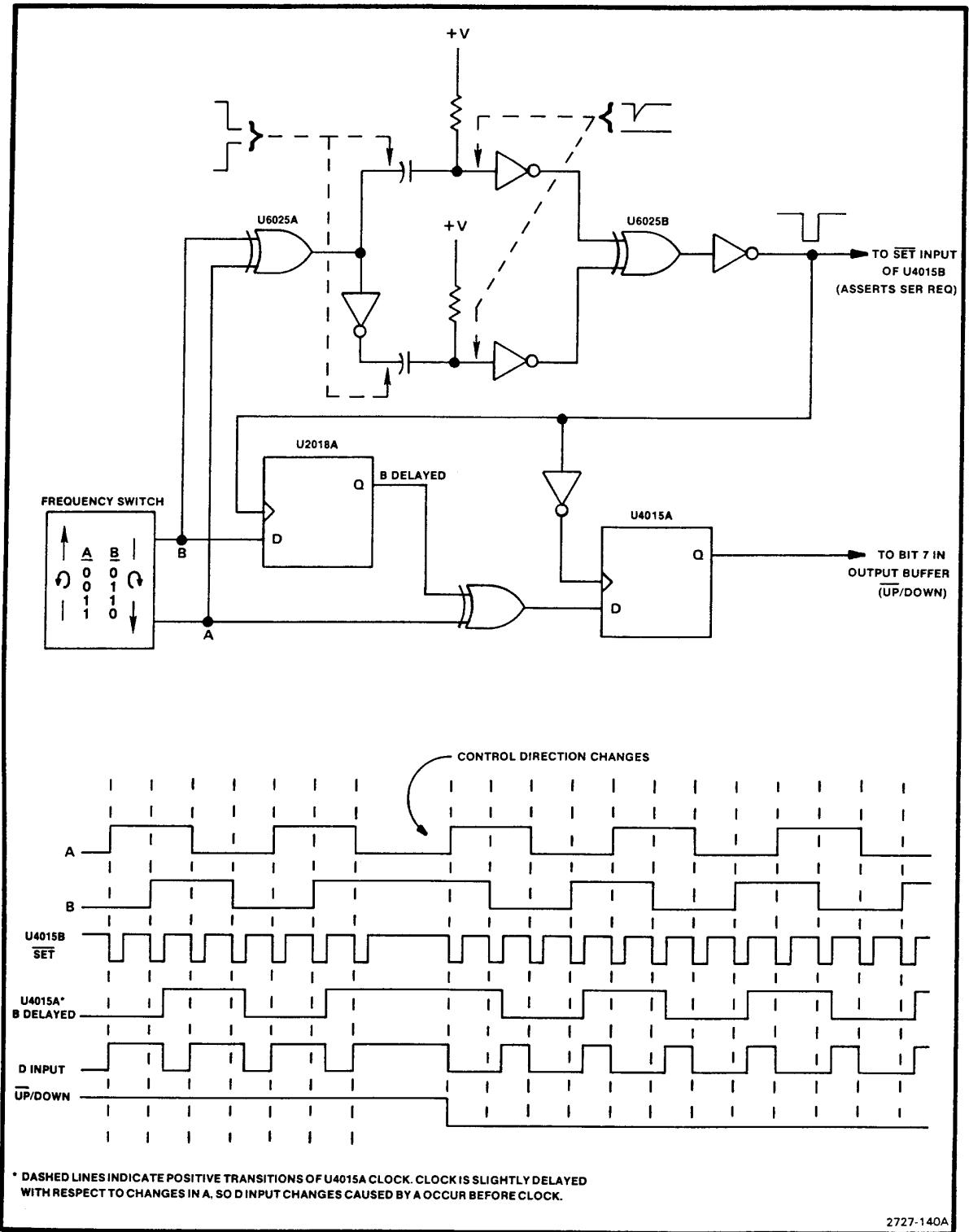HEX CODE

2727-139

Fig. 5-39. Switch matrix codes.

Fig. 5-40. Frequency control encoder timing.

INTENSITY is an input to the Z-Axis/RF Interface board to control trace brightness.

PEAK/AVERAGE is a digital storage input that causes signals to be peak detected above, and averaged below, a display line that tracks this control.

MANUAL SCAN varies the horizontal position of the sweep in manual sweep mode.

POSITION centers the sweep and vertical deflection on the crt.

LOG CAL varies the video signal level prior to the Video Processor board.

PEAKING controls front-end response of the analyzer by fine-tuning the internal preselector or varying the bias of an external mixer.

AMPL CAL adjusts 10 MHz IF gain.

ACCESSORIES INTERFACE BOARD ◈47◈

The Accessories Interface board provides access to the instrument bus and connection for two analog signals. The instrument bus access may be used for diagnostics; it may also be used by future accessories.

The analog signals are an input, EXT VID IN, and an output, EXT PRESEL. To display an external signal applied to EXT VID IN, place a TTL low on $\overline{\text{EXT VID SEL}}$. EXT PRESEL can drive an external preselector for use with an external mixer; it is available only with Option 01 and is valid only in preselector bands (1.7 GHz to 21 GHz). This signal tracks the instantaneous frequency at a nominal 2.1 GHz/volt with zero output corresponding to 2.072 GHz.

The instrument bus is buffered and brought out to the rear panel with the lines named to indicate their relation to the internal bus: ADV for DATA VALID, APOLL for POLL, etc.

Two lines are added to define the 492/external device interface. One, INTL CONT, is asserted low by an external controller to disable the internal microcomputer's instrument bus buffers. This sets the address lines buffer, U2033, and control lines buffer, U2015, to drive the address, DATA

VALID and POLL lines, and listen to $\overline{\text{SER REQ}}$. It also sets U2038 to indicate the direction of data through the data lines buffer, U2025, depending on the sense of the MSB of the address—AB7. When INTL CONT is low, it sets U2038 to drive the buffer in a manner similar to the Processor board data buffer—a write to the internal bus if AB7 is low and a read if AB7 is high. When INTL CONT is high, the buffer is enabled to write to the external bus when AB7 is low and read when AB7 is high.

The other line is asserted low by an external device to enable the data buffer. As long as this line, DATA BUS ENABLE, is unasserted, the data buffer is set to its high-impedance state and the data direction input has no effect on its output.

POWER SUPPLY ◈10◈

The Main Power Supply furnishes all the regulated voltages for the 492/492P, except for the crt high-voltage supply. In order to reduce total weight and conserve energy, the Main Power Supply is of the high-efficiency design. The power supply consists of the line input circuit, which rectifies and filters the incoming line voltage; the inverter, which drives the primary of the power transformer; the rectifier-filter circuit, which rectifies and filters the secondary voltages; the voltage reference circuit, which furnishes a stable and precise reference for the regulators; the regulator circuts, which control the voltage and current for the supplies that requires precise regulation.

The Fan Driver board houses the Fan Driver circuit, which furnishes the appropriate drive current for the fan motor. It also contains the Overvoltage Protection circuit, which shuts down the +5 V supply in case of overvoltage. Refer to Diagram 43.

MAIN POWER SUPPLY ◈43◈ ◈44◈

Line Input Circuits

Power is applied through the line filter FL301, then through the line fuse and additional normal mode/common mode EMI filtering to the power switch, from where it is sent through line selector connector J1091. The line filter prevents power line interference from entering the power supply and internally generated signals from radiating out the power cord.

Line selector connector J1091 permits the instrument to operate from either 115 V nominal or 230 V nominal line

voltage source. When J1091 is in the 115 V position (pins 1 and 2), rectifiers CR3096 and CR4094 operate in conjunction with energy storage filter capacitors C6101 and C6111 as a full-wave doubler; thus, the voltage across the two capacitors is the peak-to-peak value of the line voltage. When J1091 is in the 230 V position (pins 2 and 3), CR3096, CR4095, CR3098, and CR4094 operate as a bridge rectifier. As a result, the output voltage applied to the inverter is about the same for 115 V or 230 V operation.

Thermistors RT2093 and RT2097 limit current surge to the supply at turn-on. After the analyzer is in operation, the current demand drops, the resistance value of the thermistors drops, and they have minimum effect on the circuit.

WARNING

Because C6011 and C6101 discharge very slowly, hazardous potentials exist within the power supply for several minutes after the power switch is turned off. A relaxation oscillator, formed by C5113, R5111, and DS5112, indicate the presence of voltages in the circuit until the potential across the filter capacitors is below 80 V.

S2103 is a thermal cutout switch that opens if the interior of the instrument reaches 103°C. It prevents overheating in case the cooling fan fails.

E1094 and E2095 are surge voltage protectors. When the line selector switch is in the 115 V position, only E1094 is connected across the line input. If a peak-voltage surge in excess of 230 V occurs across the input, or if the instrument is accidently connected to a 230 V source, E1094 will break down and demand enough current to open the line fuse. When the instrument is operated with the line selector at 230 V, E1094 and E2095 operate in series to protect the input against line surges of about 460 V peak.

The voltage for the line trigger source is taken off the input circuit just past S2103. It is coupled through C3085 and C3089 then off the board to the Sweep circuit to provide instrument triggering at line frequencies. The voltage at the top of R6093 is about 2 V peak-to-peak.

Inverter Circuit

The inverter consists of several stages: a multivibrator that produces a square-wave signal to drive the ramp generator and the inverter logic circuits. The ramp generator produces a low-level sawtooth ramp that is applied to the primary regulator circuit. The inverter logic circuits control

the duty cycle of the inverter driver, and thus the inverter output stage. The primary regulator compares the +17 V supply output with a reference voltage, and gates the inverter logic circuits off and on to control the inverter duty cycle and thus the effective primary voltage. The inverter driver stage amplifies the signal from the inverter logic circuit and drives the output stage. The output stage consists of two power switching transistors that drive the primary of the main power transformer, T4071. Primary overcurrent sense and soft start circuit add protection.

Multivibrator. U6059, a low power 555 timer, is a multivibrator that operates at about 66 kHz and 80% duty cycle. Oscillator frequency is adjusted by R6061. The output square-wave signal is applied through R6052 to the primary of T6044 in the ramp generator, and directly to U6053, U6063A, U6063B, and U6069.

Ramp Generator. This circuit consists of T6044, Q5023, Q6034, and Q5032, and surrounding components. The circuit is a gated sawtooth generator that operates as follows: The negative excursion of the square-wave signal from Q6056 is coupled across T6044, forcing Q6034 into conduction. This forward-biases Q5032 and its collector moves toward +17 V, charging C5038 to this value. Shortly thereafter, Q6034 loses drive (since the pulse coupled across T6044 has died away) and the two transistors cut off. Q5023 acts as a constant-current drain to discharge C5038 linearly. This signal is coupled across divider R5036/R6032 then applied through C6039 to the input of comparator U6036, part of the primary regulator.

Primary Regulator. This circuit consists of comparator U6036 and U6046, photocoupler U6043, and related components. The circuit varies the duty cycle of the driving signal for the inverter as follows: The +17 V_1 voltage is divided by R6038 and R6037 to about +4.8 V, and applied to the inverting input of U6036. The +5 V reference is applied through R6022 to the non-inverting input of U6036, where it is combined with the ramp signal from the ramp generator stage. The non-inverting input thus receives a sawtooth signal of about 500 mV peak-to-peak imposed on +5 V dc level. This is compared with the +4.8 V on the other input, so the comparator switches with each sawtooth cycle. Now, refering to Fig. 5-41, note that as the level at pin 3 (which corresponds to +17 V supply variations) rises and falls, the duty cycle of the output waveform varies also.

The signal from the output of U6036 is applied to U6043, an optical isolator. The output of this stage is then applied to the input of U6046, a comparator. The inverting input of this device is referenced at +2.55 V, so the comparator switches at the crossing point. The purpose of the last two stages is to shift the dc level of the output signal of U6036 to CMOS levels to drive the inverter logic.
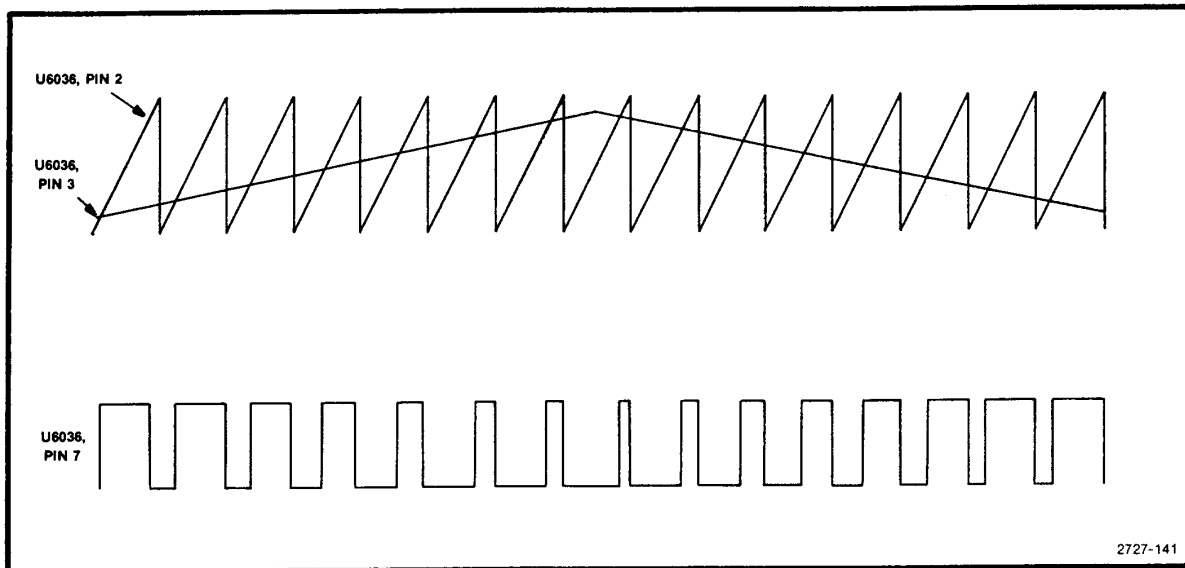
REV AUG 1981

Fig. 5-41. Primary regulator input and output waveforms (stylized).

Inverter Logic. This stage consists of steering flip-flop U6063 and dual quad-input NAND gate U6069. The flip-flop is connected so it toggles back and forth and enables first one gate then the other. The square-wave signal from the multivibrator drives the clock input of U6063; the signal also enables each gate to ready it for the other signals that arrive later. Depending on the output state of U6063, either the upper or lower section of U6069 will be ready for the enabling signal. Assume for the moment that the Q output is holding pin 2 of U6069 high. This means that the complement output of the latch is holding the opposite side of the gate pair disabled. Now, when the output of U6046 moves high (U6046 controls the duty cycle of the Inverter), the upper section of U6069 produces a low state. This causes current to flow through half the primary and Q6078 only. On the opposite cycle of the multivibrator signal, the latch is reset, the lower half of U6069 is enabled, and Q6077 is in the conduction path.

Inverter Driver. The inverter driver consists of transistors Q6077 and Q6078, transformer T6081, and related components. This is a push-pull amplifier with diode protection in the collector circuits to prevent damage from voltage transients during operation. The drive signal is induced into the two secondary windings of T6081 and coupled to the output stage.

Output Stage. This circuit consists of transistors Q2071 and Q2061, series LC tank L1081/C1063, and transformer T4071. The output transistors are connected in a half-bridge configuration, converting the previous push-pull output to a single-ended configuration. The two transistors drive the se-

ries tank which acts as an energy storage element and an averaging circuit. Output transformer T4071 is driven by the tank circuit, and in turn drives the secondary circuits.

Primary regulation, as discussed previously, is accomplished by varying the duty cycle of the main switching transistors in the inverter driver. Maximum duty cycle occurs at low input line (90 V) and fully loaded output. At maximum duty cycle, both transistors are off for only 20% of the period, or 3 μs. This short period allows any stored base charge to deplete, so there is no chance of both transistors conducting at once. Minimum duty cycle occurs at high input line (132 V) and minimum loaded output. At minimum duty cycle, each transistor is off for about 6 μs, or 40% of the total period.

Softstart and Primary Overcurrent Circuits

The soft start circuit consists of U6053 and associated components. Soft start gradually increases the switching transistor's duty cycle at turn-on or after overcurrent shutdown. This prevents excessive transistor current due to charging output capacitors. Refer to Fig. 5-42 for timing waveforms.

The primary overcurrent circuit protects against secondary shorts destroying the switching transistors. T2080 senses the collector current in Q2071 and creates a voltage on pin 5 of U6046B. If the bias on pin 5 surpasses the 2.5 V reference on pin 6, at about 5 A through Q2071, the output of U6046B sets U6063A. U6063A is a D-type flip-flop used as a timer to shut down the inverter logic for about one second. U6063A also resets the softstart circuit.
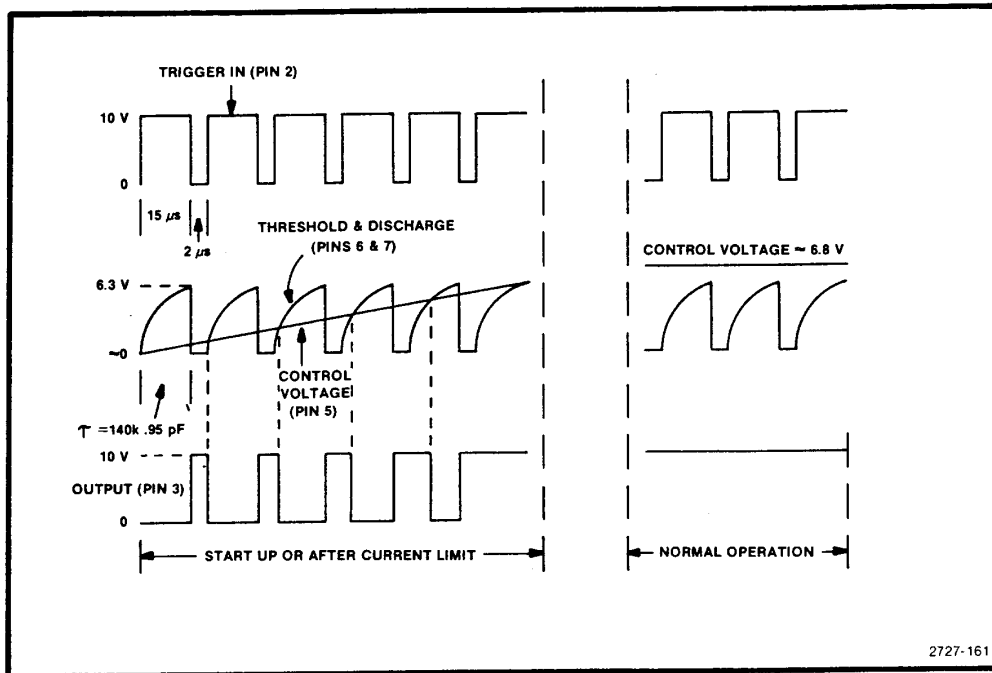
Fig. 5-42. Timing waveforms (stylized) for soft-start circuit.

Rectifier-Filter Circuits

Transformer T4071 has three secondary windings: The first furnishes current to the +300 V and +100 V supplies; the second furnishes current to the −7 V, +7 V, and +9 V supplies; and the third furnishes current to the +17 V and −17 V supplies. The regulated supplies (+5 V reference, +5 V, −5 V, +15 V, and −15 V) derive their current from the rectifier-filter circuits.

The ac voltage from pins 7 and 8 of T4071 is applied to a bridge rectifier composed of CR3053, CR3056, CR3055, and CR3054. The output of this rectifier is filtered, then applied to the remainder of the instrument as the +100 V supply.

The +300 V supply is derived by stacking a 2X multiplier on the +100 V supply. CR3052, CR1042, CR1034, and CR1022 compose this circuit.

The ac voltage from pins 9 and 10 supply current to full-wave rectifier CR4061/CR4062; its output is filtered and sent to the remainder of the instrument as the +9 V supply. Two other taps off the same winding (pins 11 and 12) supply current to the bridge rectifier that consists of CR4063, CR4057, CR4053, and CR4065. The output divides across filter capacitors C3051 and C4051, to become the +7 V

and −7 V supplies. The +7 V supply is only used on the power supply board; the −7 V supply is used by other circuits in the 492/492P.

The third winding of T4071 is pins 13, 14, and 15, which furnish current to full-wave bridge rectifier CR5052, CR5062, CR5065, and CR5055. The output of this rectifier is also divided to become the +17 V and −17 V supplies. The −17 V supply is used only on the power supply board; the +17 V supply is used both on the board and elsewhere in the 492/492P.

Voltage Reference Supply

The +17 V is fed through R6021 and R6020 to the voltage divider that feeds zener diode VR6026. The 6.2 V from the zener diode is divided across R6029, R6028, and R6023. +5 V REF adjustment R6028, is set for precisely +5 V at TP6027.

Regulator Circuits

Four of the available voltages from the power supply are regulated: +15 V, −15 V, +5 V, and −5 V. In function, all four regulators are the same. The circuit differences are minimal so only the +5 V regulator is discussed here. Significant differences are discussed following this description.

The voltage regulator part of the circuit is U2037A which compares the +5 V REF and +5 V SENSE voltages, amplifies the difference, and applies the change to Q2023, the driver transistor. The change is amplified by this stage and applied to the base of series-pass transistor Q2024 changing its conduction to correct for the original change to the +5 V.

The current regulator portion of the circuit is U2037B. A change in current through R2017 is applied to the non-inverting input of U2037B, which amplifies the change and applies it to the base of the driver transistor Q2023. The transistor amplifies the change which alters the bias of Q2024, causing it to restore the current flow through R2017 to its former value.

The +15 V regulator is the same as the +5 V regulator, except that the coupling circuits from the preamplifiers are separated from one another. The −15 V regulator is virtually identical to the +5 V regulator. The −5 V regulator differs from the others in that a driver stage is not required, so the preamplifiers drive the series-pass transistor (Q5013) directly.

Over-voltage Protection Circuit

Zener diode VR1015 and SCR Q1010 form the over-voltage protection circuit. If the +5 V supply passes +6 V, the potential on the gate of Q1010 biases it into conduction. This forces the +5 V supply to ground; it remains at ground potential until the analyzer is de-energized and turned on again.

Fan Drive Circuit

The Fan Drive circuit provides a temperature-controlled current drive to the fan motor. The circuit produces a three-phase drive current of approximately 240 Hz operating frequency. The actual drive circuit operates as a ring counter.

Transistors Q1038 and Q1044 form a current regulator that is controlled by thermistor RT2045, the value of which varies inversely with the internal temperature of the analyzer. The thermistor and a companion resistor R2042, fix the voltage at the emitter of Q1044 at about −13 V at turn-on, and more positive as the analyzer warms up.

The ring counter consists of three stages: Q1025 and Q1020, with R1031/C1032 and R1027/C1018 as the frequency-determining components; Q2025 and Q1018, with R1033/C1033 and R2019/C1019 as the frequency-determining components; and Q2030 and Q2020 with R2014/C2012 and R2016/C2018 as the frequency-determining components. When the analyzer is energized, one of

the three ring counter stages begins conducting before the others, owing to circuit imbalances. Assume that the upper stage (Q1025 and Q1020) begins conducting before the others. The collector voltage of Q1025 is near −17 V which fixes that point as the most negative in a ring consisting of R1032, R1029, R1028, R2036, R2034, and R1036. Since the emitter voltage of the three control transistors (Q1020, Q1018, and Q2020) is the same, the voltage division around the resistive ring is such that Q1018 and Q2020 remain cut off. When the capacitive charge that holds Q1020 in conduction bleeds off, the transistor cuts off and the next stage can begin to conduct. The remaining two are in turn prevented from operating until the RC combination discharges. The fan motor inductance works in conjunction with the RC components to regulate the switching of the stages.

This ring-counter action builds up slowly until the circuit is producing a three-phase drive signal of about 240 Hz. The inductance of the motor coils round off the otherwise sharp corners of the driving signal, so the current waveform looks a great deal like the output of a half-wave rectifier at P2020, pins 1, 2, and 3. Each of the driving signals are approximately 120° apart, so as to drive the motor.

The rackmount/benchtop versions require an external fan, B200. When this fan is connected, the internal fan (B100) is disconnected.

492P GENERAL PURPOSE INTERFACE BUS ◇48◇

The 492P, unlike the 492, includes GPIB capability provided by two boards: the GPIB board and the GPIB Interface board. The GPIB board contains ROM and RAM used by interface functions and the interface between the microcomputer and the GPIB. The GPIB Interface board holds the GPIB buffers and address switches.

Address Decoding

RAM. RAM on the GPIB board supplies I/O buffer space for GPIB transfers. The RAM ICs, four bits wide, are paired to make 8-bit bytes at each address. For instance, U1032 and U1042 are both selected when HIRAM is asserted. The 10 lower bits on the address bus select an address cell within each IC. The RAM address range, 800 to 1000 (hex), is decoded by half of U1028. Either RAM select line is enabled by GPIBRAM from the Processor board and the state of A10 on the address bus.

GPIB Interface and Address Switch Register. Either the GPIB interface (U2047) or the address switch register (U3039) is selected by the other half of U1028. The select line for either is enabled by GPIA from the Processor board

and chosen by A3. When A3 equals 0, it selects the GPIB interface; when A3 equals 1, it selects the switch register. The GPIB interface is described below. The address switch register is a buffer, U3039, for the rear-panel GPIB AD-DRESS, LF OR EOI, TALK ONLY, and LISTEN ONLY switches.

ROM. ROM on the GPIB board contains the portion of the instrument operating system that handles GPIB data transfers. This portion of the firmware decodes and responds to messages received on the bus, transferring control to the appropriate subroutines in Memory board firmware to execute the actions called for by the message.

The ROM address space is divided into two banks, either of which can be filled with four 2k packages or a single 8k package. Straps on the board are set to control decoder U1021 and to route signals as needed to match the ICs that are installed. For 2k ROMs, U1021 decodes A11 through A13 to assert one of its eight chip-enable outputs during a read cycle within the ROM address range (4000—8000, i.e., A14 high and A15 low). For 8k ROMs, U1021 decodes only A13 to assert either its Y0 or Y4 output. Straps on U2012 and U3012 inputs are set to apply the correct enable and address signals for either kind of ROM.

GPIB Interface

The GPIB interface is based on the 9914 general purpose interface adapter (GPIA). U2047, the GPIA, performs the majority of the functions specified in IEEE Standard 488-1978 and allows firmware implementation of the rest of those functions. These functions are not explained here, but are discussed in some detail in an appendix in the 492P Programmer's manual.

The GPIA's internal logic handles:

Source and acceptor handshakes
Talker and listener functions
Recognizing GPIB address
Service request (SRQ)
Remote/local function
Local lockout
Serial and parallel poll response
Respond to device clear
Respond to device trigger
NRFD holdoff when receiving data

GPIA Block Diagram

The bus and register organization of the GPIA is shown in Fig. 5-43. The 13 registers are the vehicles used for communication between the 492P microcomputer and the GPIB. Some registers provide a link between the microcomputer and GPIB; others are used by the microcomputer to control the GPIA and obtain status information.

The registers are addressed by signal lines RS0 through RS2 and the DBIN input (connected to the microcomputer read/write line): DBIN high selects read registers, DBIN low selects write registers. The registers are shown in Table 5-25.

Two interrupt status registers keep track of changes that may require microcomputer attention: data byte received or sent, EOI, GET, DCL, or IFC received, a remote/local state change has occurred, and ATN going false are examples. Corresponding interrupt mask registers are set by the microcomputer to control interrupt status results in an interrupt.

The address status register indicates the remote/local state of the GPIA, the state of ATN, and the listener/talker addressed states. The bus status register reflects the current state of GPIB bus management lines.

The auxiliary command register receives commands that control chip functions and local messages to the GPIA functions (such as rtl—return to local).

The address register contains the instrument's primary address.

The serial poll register contains the status byte.

The command pass-through register connects the GPIB data lines to the microcomputer data lines to transfer commands not automatically handled by the GPIA.

The parallel poll register is used by the microcomputer to respond to a parallel poll.

The data-in and data-out registers are the route for data transferred between the microcomputer bus and the GPIB when the instrument is either addressed as a listener or talker. The 9914 automatically asserts NRFD until the microcomputer reads the data-in register.

GPIB Buffers. Two transceivers on the GPIB Interface board buffer signals on the GPIB.

The data bus buffers, in U1012, are controlled by two signals: TE (talk enable) and PE (pull-up enable). TE from the GPIA sets the direction of data flow: high means GPIA to GPIB and low GPIB to GPIA. PE low disables the driver pull-ups for open collector operation when ATN is asserted; this disables tri-state operation, which is required during a parallel poll (when ATN is asserted).
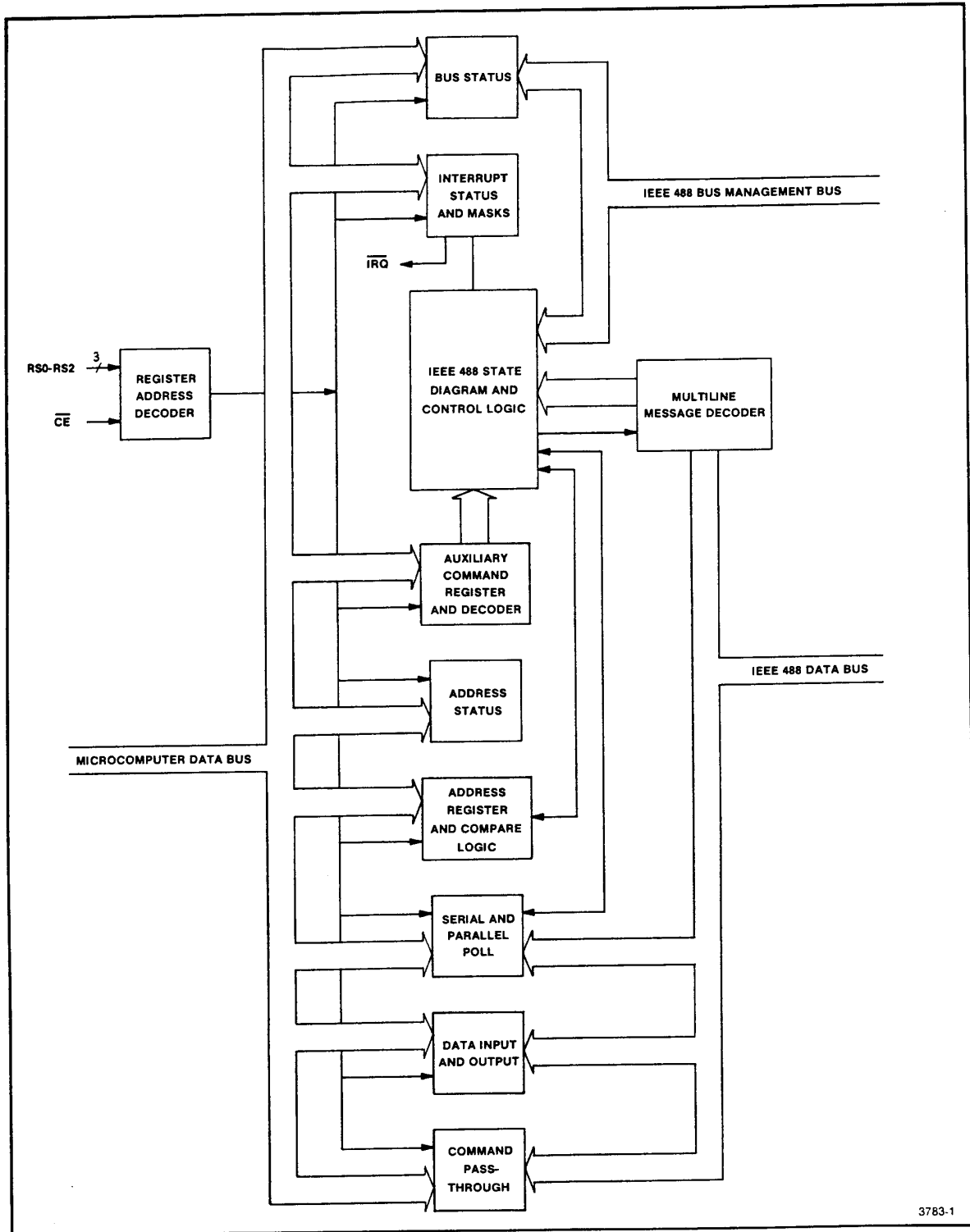
Fig. 5-43. 9914 GPIA block diagram.

Table 5-26
GPIA REGISTERS

Register	Type	RS2	RS1	RS0	DBIN & WE
Interrupt Status 0	Read	0	0	0	1
Interrupt Mask 0	Write	0	0	0	0
Interrupt Status 1	Read	0	0	1	1
Interrupt Mask 1	Write	0	0	1	0
Address Status	Read	0	1	0	1
Bus Status	Read	0	1	1	1
Auxiliary Command	Write	0	1	1	0
Address Switch	Read	1	0	0	1
Address	Write	1	0	0	0
Serial Poll	Write	1	0	1	0
Command Pass Through	Read	1	1	0	1
Parallel Poll	Write	1	1	0	0
Data In	Read	1	1	1	1
Data Out	Write	1	1	1	0

The bus management buffers in U1011 are automatically configured by TE and ATN to operate in the required direction (driving DAV and EOI when TE is high and NDAC and NFRD when TE is low).

RACKMOUNT/BENCHTOP VERSIONS
OPTIONS 30, 31, AND 32
OF 492/492P

Introduction

The rackmount version of the 492/492P Spectrum Analyzer (Option 30) is designed to mount in a standard 19-inch rack. The benchtop version (Option 32) is the same as the rackmount except it has side panels with handles and it also has feet installed on the bottom. Both have a larger fan to provide additional cooling. Option 31 provides access to all front-panel connections via the cabinet rear panel.

This section describes characteristics of the rackmount/benchtop versions, mounting procedure, and servicing procedures for the rackmount/benchtop instruments.

Electrical Characteristics

Electrical characteristics for the 492/492P are applicable for the rackmount/benchtop version of the 492/492P except residual (FM'ing) response, and frequency response, when Option 31 is included. Rackmount versions, subject to externally induced vibrations from rack cooling fans or the surrounding equipment, may show degradation of the FM'ing characteristic. Because of different rack configurations, this degradation cannot be specified. In a typical fan-cooled rack, degradation increases by a factor of two.

Frequency response and display flatness performance, for Option 31 installation, typically degrades up to 2 dB in the negative direction, above 3.0 GHz.

Table 6-1
ENVIRONMENTAL CHARACTERISTICS

Rackmount versions meet MIL T-28800B, type III, class 5, style F specifications. Benchtop version meets MIL T-28800B, type III, class 5, style E specifications. Some of the details are as follows:

NOTE

For vibration, shock, and bench handling tests, the semi-rigid cables between the front-panel connectors and the front-grill connectors (for Option 31) must be removed. The bail for tilting the benchtop version (Option 32) must be folded.

Characteristics		Description
Temperature and Humidity	Temperature °C	Relative Humidity %
Operating	0 to 25	95 +5, −0
	25 to 40	75 ±5
	40 to 50	45 ±5
Non-operating	−55 to 75	95 +5, −0
Altitude		
Operating	10,000 feet	
Non-operating	40,000 feet	

Table 6-1 (cont)

Characteristics	Description
Vibration	
Operating	Method 514 Procedure X (modified MIL-STD-810C). Vibration limit is 1 G. Resonance searches along all three axes at .0065 inch; frequency varied from 10 to 55 Hz, 15 minutes per axis, plus dwell at resonant frequency of 33 Hz for 10 minutes per axis. Total vibration time 75 minutes. Instrument secured to rack or vibration platform during test.
Shock	For Option 31, the semi-rigid coaxial cables running from the front panel to the rackmount cabinet grill must be removed for this test.
Transit Drop	Not applicable.
Bench Handling	The bail for tilting the instrument shall be folded and the semi-rigid cables from the front-panel connectors to the front grill connectors (Option 31) shall be removed for this test.
Transportation	
Package vibration	Meets National Safe Transit Association's pre-shipment test (project 1A-B-1) when correctly packaged. One hour vibration of 1 G.
Package drop	Operable after a 24-inch drop on any corner or flat surface.

Table 6-2
PHYSICAL

Characteristic	Description
Weight (standard accessories except manuals)	70 pounds maximum rackmount version and 68 pounds for benchtop version.
Dimensions	
Rackmount (without side rails)	8.75 X 16.89 X 25.00 inches (22.23 X 42.9 X 63.5 cm)
Benchtop (with feet and handles)	9.25 X 17.9 X 25.00 inches (23.5 X 45.47 X 63.5 cm)
Benchtop (without feet or handles)	8.75 X 16.89 X 25.00 inches (22.23 X 42.90 X 63.5 cm)

STANDARD ACCESSORIES

Standard accessories are the same as the 492/492P with the addition of rack slides for the rackmount (Tektronix Part No. 351-0375-01). An accessories drawer provides storage space in place of the front cover. Option 31 includes semi-rigid cabling to connect the front-panel connectors to the cabinet rear connectors; and a front-panel grill.

OPTIONAL ACCESSORIES

Same as the 492/492P except for the transit case

RACKMOUNTING INSTALLATION DIMENSIONS

Height. At least nine inches of vertical space is required to mount this instrument in a cabinet rack.

Width. Minimum width of the opening between the left and right front rails of the rack must be 17.9 inches. This allows room on each side of the instrument for the slide-out tracks to operate freely, permitting the instrument to move smoothly in and out of the rack.

Depth. The rackmount version requires 25 inches behind the front rails for air circulation, power cord, and the necessary mounting hardware.

SLIDE-OUT TRACKS

WARNING

If the left and right slide-out tracks are reversed, the safety latch can be defeated, allowing the instrument to be pulled out of the rack. When mounting the slide-out tracks, differentiate the left assembly from the right and mount only as directed in these instructions.

The hardware provided for mounting the slide-out tracks is shown in Fig. 6-1. Since the hardware is intended to make the tracks compatible with a variety of cabinet racks and installation methods, only part of the hardware will be needed for this installation.

Figure 6-2 shows the rackmount version installed in a cabinet-type rack. The slide-out tracks provided permit it to be extended out of the rack for access to the back connectors. To operate in the extended position, be sure the power cord and any interconnecting cables are long enough for this purpose.

The slide-out tracks consist of two assemblies—one for the left side of the instrument and one for the right side. Figure 6-3 shows the complete slide-out track assemblies. The stationary section of each assembly attaches to the front and rear rails of the rack, and the chassis section is attached to the instrument. The intermediate section slides
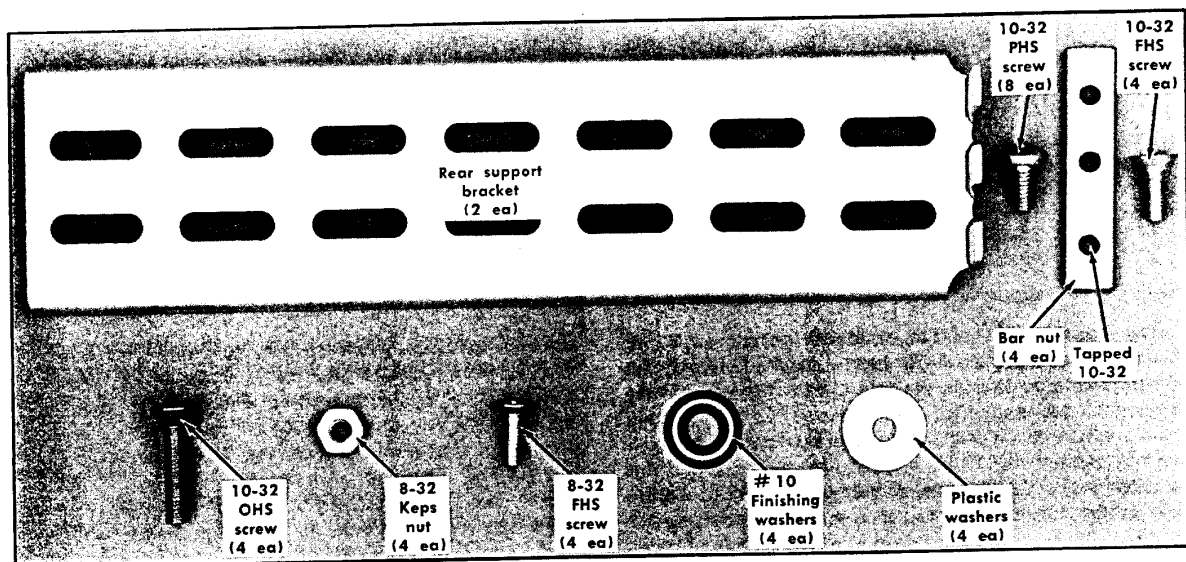
Fig. 6-1. Hardware provided for slide track mounting.
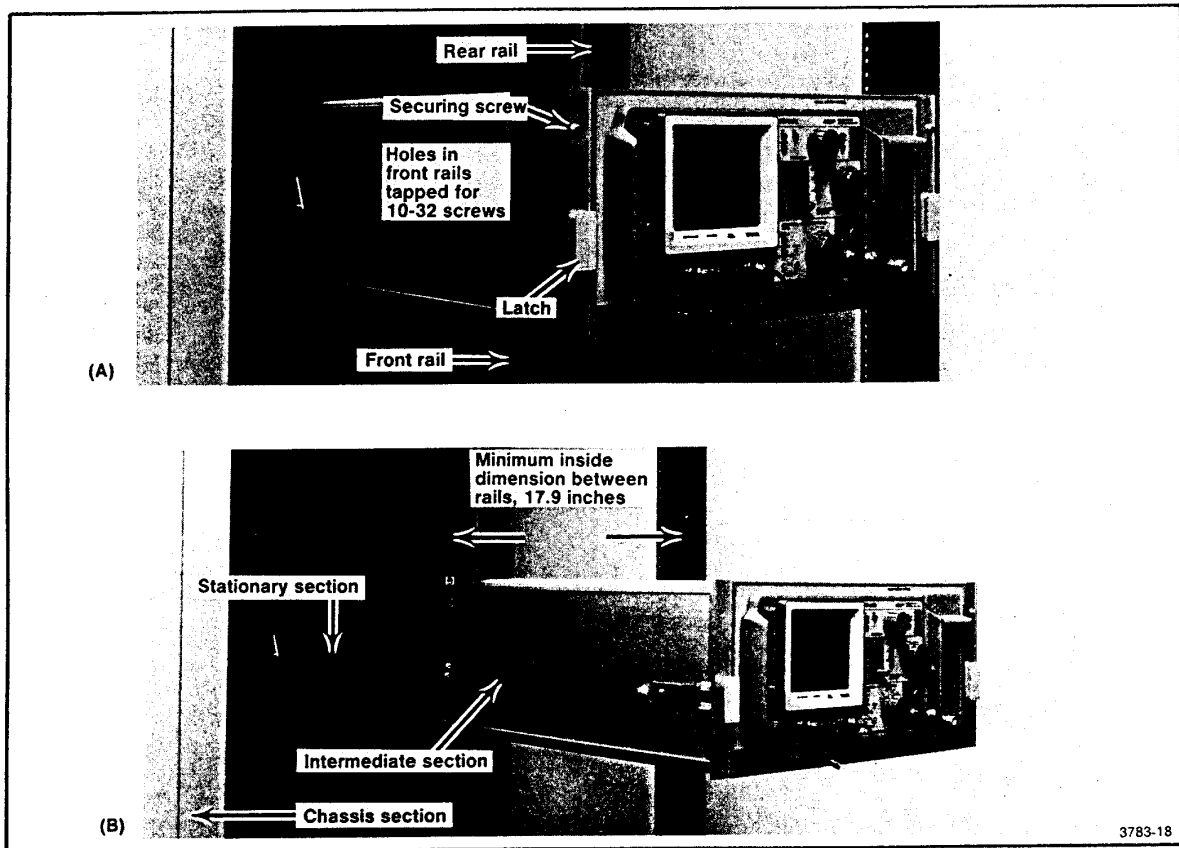
Fig. 6-2. Instrument installed in a cabinet-type rack.

between the stationary and chassis sections and allows the instrument to be extended out of the track. *When the instrument is shipped, the stationary and intermediate sections of the tracks are packaged as matched sets and should not be separated.* To identify the left or right assembly note the position of the automatic latch (see Fig. 6-3). When mounted in the rack, the automatic latch should be at the top of both assemblies. The chassis sections are installed on the instrument at the factory.

Mounting Procedure

The front flanges of the stationary sections may be mounted in front of (outside) or behind (inside) the front rails of the rack, depending on the type of rack. If the front rails of the rack are tapped for 10-32 screws, the front flanges are mounted outside of the rails. If the front rails of the rack are not tapped for 10-32 screws, the front flanges are mounted inside the front rail and a bar nut is used. Figure 6-4 shows these methods of mounting the stationary sections.

Use the following procedure to install the rackmount version in a rack:

1) select the proper front-rail mounting holes for the stationary sections, using the measurements shown in Fig. 6-5;

2) if the mounting flanges of the stationary sections are to be mounted in front of the rails (rails tapped for 10-32 screws), mount each stationary section as shown in Fig. 6-4A;

3) if the mounting flanges of the stationary sections are to be mounted behind the front rails (rails not tapped for 10-32 screws), mount each stationary section as shown in Fig. 6-4B;

4) refer to Fig. 6-6 to insert the instrument into the rack. Do not connect the power cord or install the securing screws until all adjustments have been made;
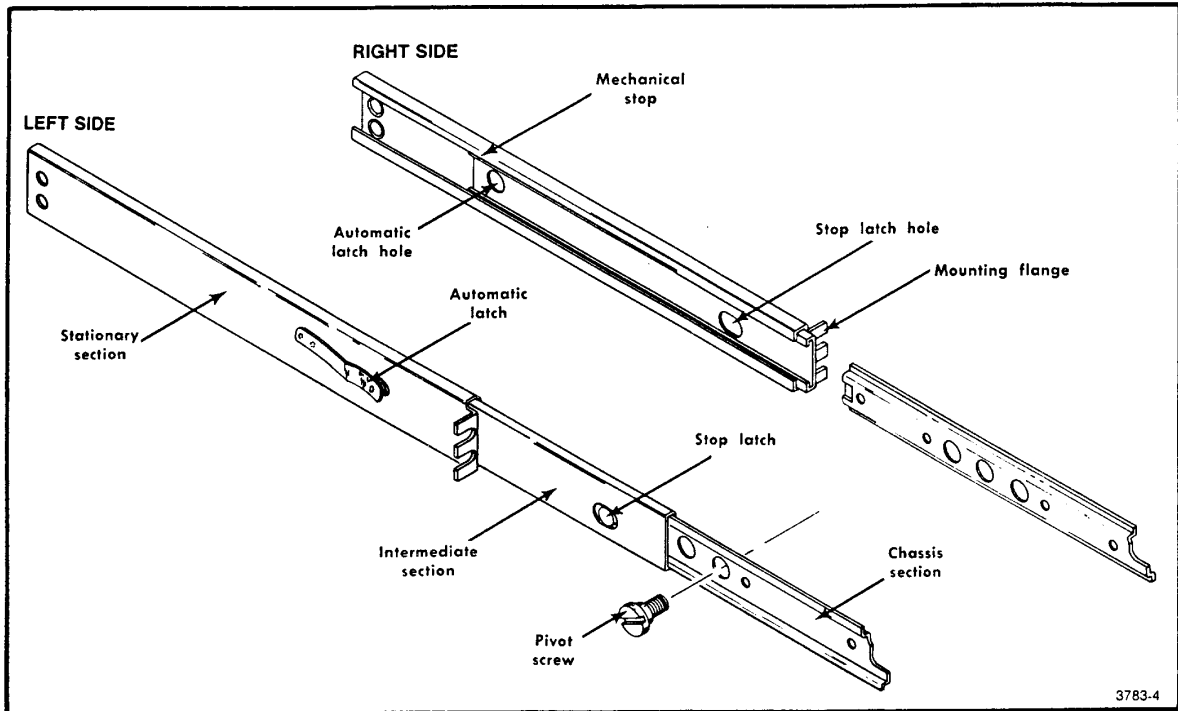
Fig. 6-3. Complete slide-out track assemblies.

5) position the instrument so the pivot screws (widest part of instrument) are approximately even with the front rails;

6) adjust the alignment of the stationary sections according to the procedure outlined in Fig. 6-7;

7) after the tracks operate smoothly, connect the power cord to the power source;

8) push the instrument fully into the rack and latch.

9) Instruments are shipped with vinyl trim strips on the cabinet flange. These strips cover two holes in the flange that can be used to insert screws to secure the rackmount cabinet to the rack frame. If you need the rackmounted instrument secured better than the latches on each side provide, cut out the vinyl cover around the hole with a sharp knife. Install the securing screws as shown in Fig. 6-2A.

CAUTION

If the rackmount version is extended out of the rack and tipped up to gain access to the bottom or back panels of the instrument, it can swing past center and fall back into the rack unless it is held. Use care when doing this to avoid damaging the front panel or equipment that may be mounted above the 492/492P.

Alternate Rear Mounting Methods

CAUTION

The following methods provide satisfactory mounting under normal conditons; however, they do not provide solid support for the rear of the instrument. If the instrument should be subjected to severe shock or vibration consult your local Tektronix Field Engineer for better rear support mounting information.
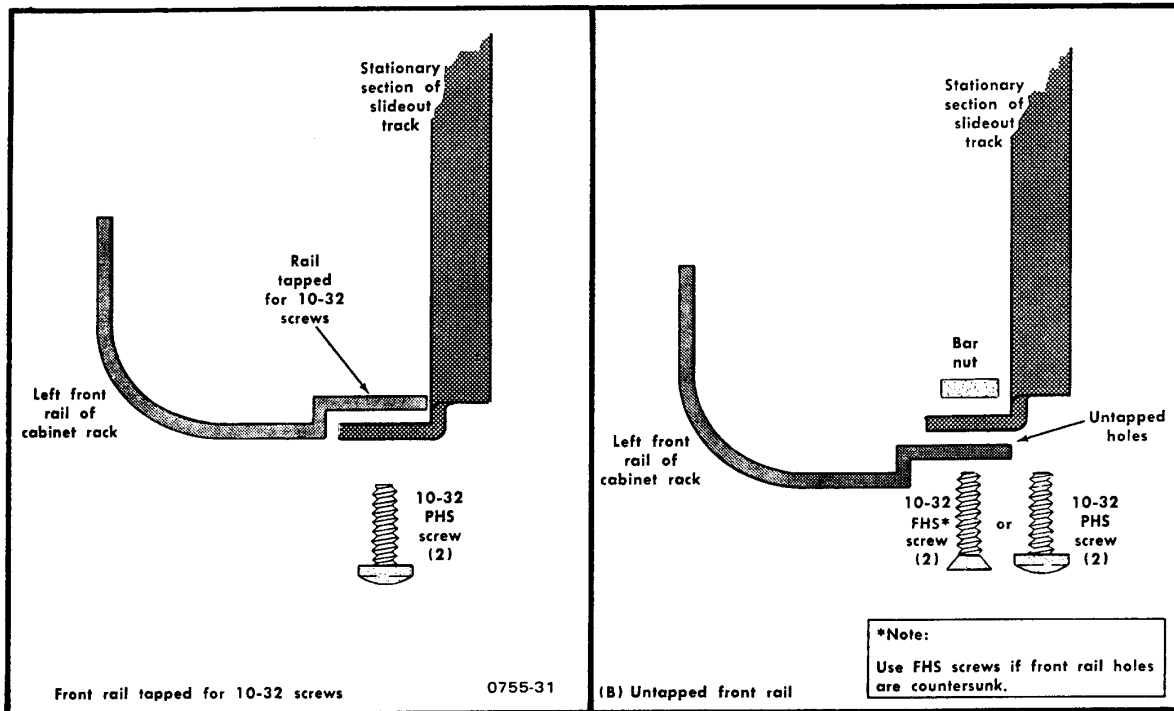
Fig. 6-4. Methods of mounting the stationary sections.

An alternative support method for the rear of the instrument is shown in Fig. 6-8. The rear support brackets, supplied with the instrument, are to be used in a rack which has a spacing between the front and rear rails of 11 to 24 inches. Figure 6-8A illustrates the mounting method if the rear rails are tapped for 10-32 screws and Fig. 6-8B illustrates the mounting method if the rear rails are not tapped for 10-32 screws.

If the rack does not have a rear rail, or if the distance between the front and rear rails is too great, the instrument may be mounted without the use of the slide-out tracks. Fasten the instrument to the front rails of the rack with the securing screws. This mounting method should be used only if the instrument will not be subjected to shock or vibration and it is installed in a stationary location.

Slide-out Track Lubrication

The special finish on the sliding surfaces of the tracks provide permanent lubrication. However, if the tracks do not slide smoothly even after proper adjustment, a thin coating of paraffin rubbed onto the sliding surfaces may improve operation.

Removing or Installing the 492/492P Spectrum Analyzer from or in the Rackmount Cabinet

After the initial installation and adjustment of the slide-out tracks, the 492/492P is removed or installed by following the directions in Fig. 6-6 and the following procedure:

1) remove the rackmount instrument from the rack and place it on a bench;

2) at the rear of the instrument, remove the Phillips screws that hold the blower assembly on the back of the 492/492P and pull the assembly off;

3) use a 5/32 Allen wrench to loosen and remove the four screws that secure the rear panel of the 492/492P to the back of the rackmount cabinet;

4) push or pull the instrument from the rackmount cabinet;

5) before the 492/492P will operate, a cut-off switch must be closed. This is accomplished by reinstalling the blower assembly on the back panel of the 492/492P.

4 1/8 inch minimum

Left front rail

Securing
holes
(tapped for
10-32 screws)

Mounting
holes

1/2 inch (for correct
position of
securing holes)

4 1/8 inch minimum

3783-6
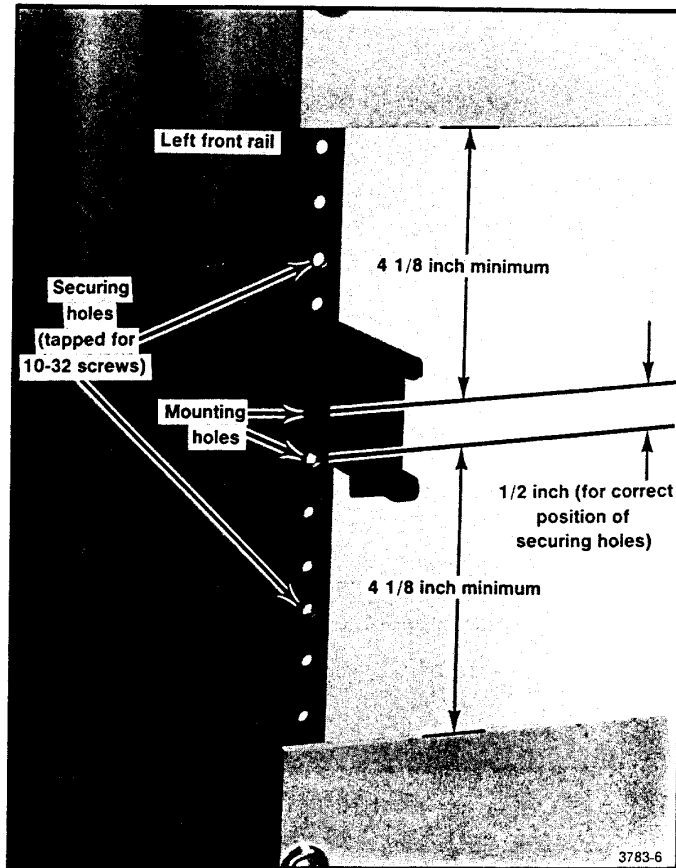
Fig. 6-5. Measurements of front-rail mounting holes for the stationary sections.

Removing the Side, Top, and Bottom Panels

1. Use a Torx "T20" screwdriver to remove the fillister screws that hold the back feet on all four corners.

2. On the side panels of the rackmount cabinet, remove the pivot and stop screw for the side rail track assembly.

3. Slide the panel back and off the cabinet. Note: When replacing the panels, be sure to start the EMI strip under the panel before sliding the panel forward; otherwise, the panel will catch the strip and bend the end. Use a pointed object such as a screwdriver to push the end of the EMI strip down while pushing the panel forward.

4. The EMI strip can be replaced by removing the back feet mounting plate and sliding the strip out of its channel.

Installing Semi-rigid Coaxial Cables that Access the Cabinet Rear Panel Connectors to the Front Panel of the Instrument (Option 31)

1. Remove the 492/492P instrument from the cabinet, then slide the bottom panel off as per instructions on removing the panels.

2. To gain access to the mounting nuts that hold the front panel grill in place, remove the horizontal support bar across the front section of the cabinet.

3. Remove the front panel grill and install the Option 31 grill. (Option 31 panel has punched openings for mounting the coaxial SMA connectors.)

4. Install the four SMA coaxial connectors in the new grill.

TO INSERT THE 492:

1. Pull the intermediate section of each slideout track out to its fully extended position.

2. Insert the chassis sections (on instrument) into the intermediate sections.

3. Press both stop latches and push the instrument into the rack until the latches snap into the stop latch holes.

4. Connect the power cord between the instrument and the power source. Connect the coaxial cables to their respective connections.

5. Again, press the stop latches and push the instrument all the way into the rack.

6. To secure the 492 to the rack, insert the 2 securing screws (with finishing washers and teflon washers) through the slots in the instrument front panel and screw them into the front rails of the rack.

TO REMOVE THE 492:

1. Remove the securing screws and washers.

2. Pull the instrument outward until the stop latches snap into the stop latch holes.

3. Disconnect the power cord.

4. Press both stop latches and pull the instrument out of the rack.

3783-20

Fig. 6-6. Procedure for inserting or removing the instrument.

5. Position the cables with RF connectors in their appropriate back panel access hole. Install the mounting nuts for each connector and secure.

6. Connect the semi-rigid cables to the SMA connector, mounted in the front panel grill, and tighten to 8 to 10 inch pounds.

CAUTION

Do not overtighten coaxial connectors beyond the recommended 8 to 10 inch pounds torque. Use a second wrench to hold the connector or cable nut as the other nut is tightened.

7. Attach the cable clamps to hold the cables to the mounting posts on the bottom of the instrument housing.

TO ADJUST ALIGNMENT:

1. Position the instrument with the pivot screws approximately even with the front rails.

2. Loosen the mounting screws at the front of both stationary sections (left side shown).

3. Allow the tracks to seek their normal positions with the instrument centered in the rack.

4. Tighten the mounting screws.

5. Push the instrument all the way into the rack. If tracks do not slide smoothly, check for correct spacing between the rear supports.

6. Check the vertical positioning of the 492 front panel with respect to adjacent instruments or panels. If not correct, reposition as necessary.

Stop screw

3783-17

Fig. 6-7. Alignment adjustment for correct operation.

8. Reinstall the support brace across the bottom of the cabinet, then reinstall the bottom panel.

9. Reinstall the instrument in the rack and install the semi-rigid cables between the front-panel connectors and the connectors on the cabinet grill.
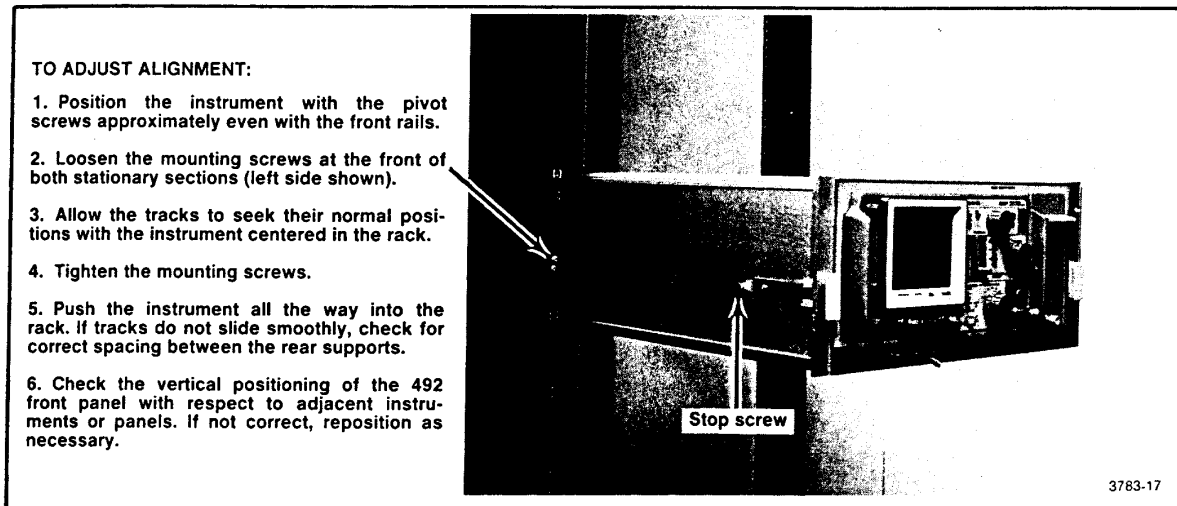
a. Ensure that the plugs and receptacles are clean and free of any foreign matter.

b. Insert the plug connectors fully into the receptacle. The length of the cables is almost the same so do not force a cable in place if it does not fit.

c. Screw the nut on finger tight to ensure it is not cross-threaded.

d. Use a 5/16 inch open-end wrench to tighten the nut to 8 to 10 inch pounds torque.

PREPARING THE INSTRUMENT FOR CALIBRATION OR MAINTENANCE

Before the 492/492P instrument can be removed from the rackmount/benchtop cabinet, the fan must be removed. After the instrument is removed from the cabinet the fan must be reconnected before power can be applied and the instrument turned on.

Prepare the instrument for maintenance as follows:

1) if the instrument is rackmounted and has the semi-rigid cables to the back panel (Option 31), disconnect the instrument semi-rigid cables between the 492/492P front panel and the connectors on the front grill of the cabinet;

2) disconnect all external connections to the instrument, including the power cord, and remove the rackmounted 492/492P;

3) place the rackmount/benchtop instrument on its face;

4) loosen the two fan assembly mounting screws and remove the fan assembly;

5) use a 5/32-inch Allen wrench to loosen and remove the four screws that hold the instrument to the cabinet back panel;

6) carefully align the fan assembly power connector pins to the receptacle on the back panel of the instrument and reinstall the fan assembly. Reconnect the power cord;

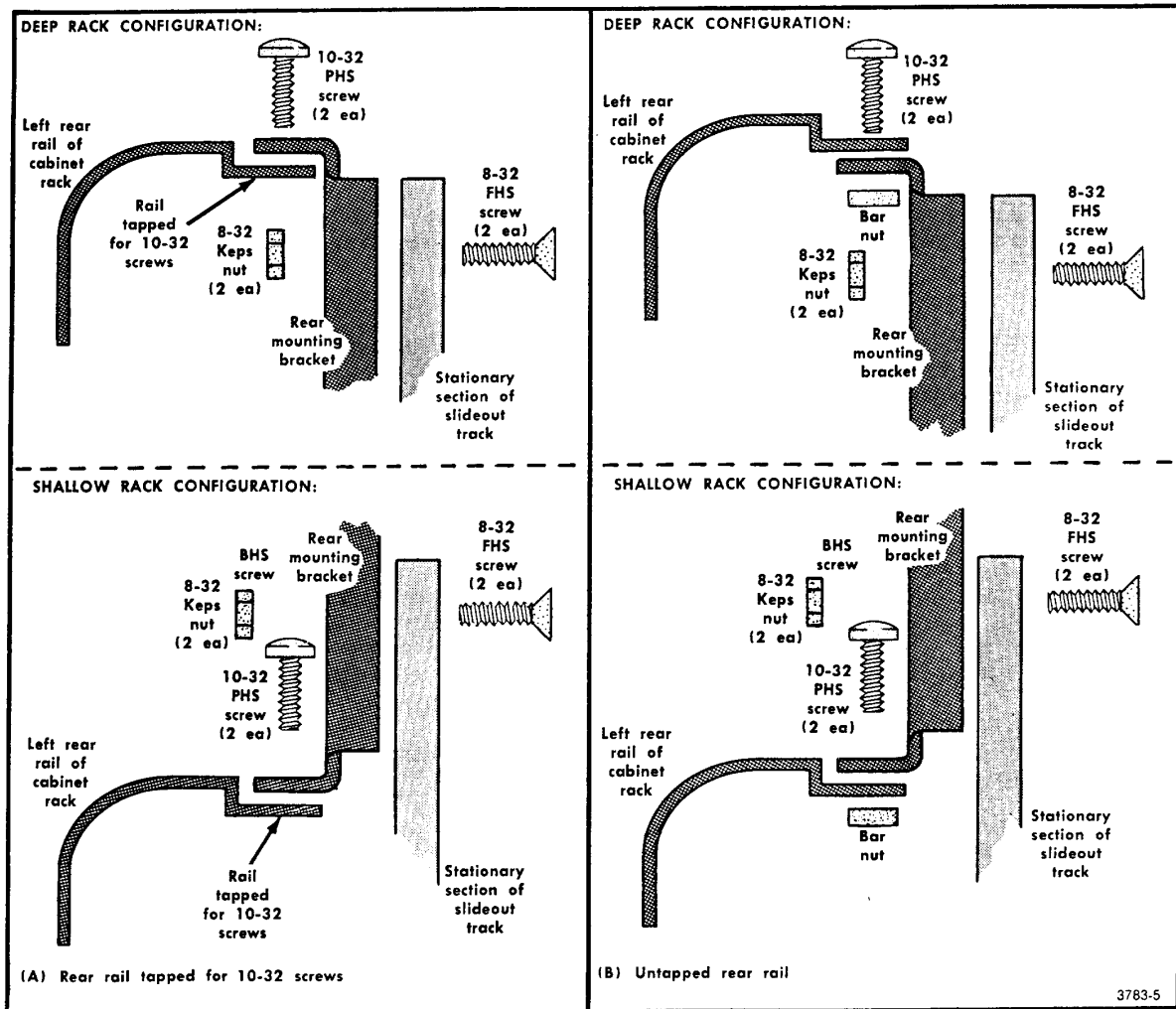7) the instrument is now ready for calibration or repair.

Fig. 6-8. Alternative method of installing the instrument using rear support brackets.

GLOSSARY

The following glossary is presented as an aid to better understand the terms as they are used in this document and with reference to spectrum analyzers.

GENERAL TERMS

Spectrum Analyzer. An apparatus which is generally used to display the power distribution of an incoming signal as a function of frequency.

NOTE

It is useful in analyzing the characteristics of repetitive electrical waveforms in general, since repetitively sweeping through the frequency range of interest will display all components of the signal.

Center Frequency. That frequency which corresponds to the center of a frequency span, expressed in hertz.

dBc. dB below carrier level.

Effective Frequency Range. That range of frequency over which the instrument performance is specified. The lower and upper limits are expressed in hertz.

Frequency Band. A part of effective frequency range over which the frequency can be adjusted, expressed in hertz.

Full Span (Maximum Span). A mode of operation in which the spectrum analyzer scans an entire frequency band.

Zero Span. A mode of operation in which the frequency span is reduced to zero.

Envelope Display. The display produced on a spectrum analyzer when the resolution bandwidth is greater than the spacing of the individual frequency components.

Line Display. The display produced on a spectrum analyzer when the resolution bandwidth is less than the spacing of the signal amplitudes of the individual frequency components.

Line Spectrum. A spectrum composed of signal amplitudes of the discrete frequency components.

Maximum Safe Input Power

WITHOUT DAMAGE. The maximum power applied at the input which will not cause degradation of the instrument characteristics.

WITH DAMAGE. The minimum power applied at the input which will damage the instrument.

Intermodulation Spurious Response (Intermodulation Distortion). An unwanted spectrum analyzer response resulting from the mixing of the nth order frequencies, due to non-linear elements of the spectrum analyzer, the resultant unwanted response being displayed.

Baseline Clipper (Intensifier). Increasing the brightness of the signal relative to the baseline portion of the display.

Pulse Stretcher. A pulse shaper that produces an output pulse, whose duration is greater than that of the input pulse, and whose amplitude is proportional to that of the peak amplitude of the input pulse.

Signal Identifier. A means to identify the spectrum of the input signal when spurious responses are possible.

Video Filter. A post detection lowpass filter.

Scanning Velocity. Frequency span divided by sweep time and expressed in hertz per second.

TERMS RELATED TO FREQUENCY

Display Frequency. The input frequency as indicated by the spectrum analyzer and expressed in hertz.

Frequency Span (Dispersion). The magnitude of the frequency band displayed, expressed in hertz or hertz per division.

Frequency Linearity Error. The error of the relationship between the frequency of the input signal and the frequency displayed (expressed as a ratio).

Frequency Drift. Gradual shift or change in displayed frequency over the specified time due to internal changes in the spectrum analyzer, and expressed in hertz per second, where other conditions remain constant.

Residual FM (Incidental FM). Short term displayed frequency instability or jitter due to instability in the spectrum analyzer local oscillators, given in terms of peak-to-peak frequency deviation and expressed in hertz or percent of the displayed frequency.

Impulse Bandwidth. The displayed spectral level of an applied pulse divided by its spectral voltage density level assumed to be flat within the pass-band.

Static (Amplifier) Resolution Bandwidth. The specified bandwidth of the spectrum analyzer's reponse to a cw signal, if sweep time is kept substantially long.

NOTE

This bandwidth is the frequency separation of two down points, usually 6 dB, on the response curve, if it is measured either by manual scan (true static method) or by using a very low speed sweep (quasi-static method).

Shape Factor (Skirt Selectivity). The ratio of the frequency separation of the two (60 dB/6 dB) down points on the response curve to the static resolution bandwidth.

Zero Pip (Response). An output indication which corresponds to zero input frequency.

TERMS RELATED TO AMPLITUDE

Deflection Coefficient. The ratio of the input signal magnitude to the resultant output indication.

NOTE

The ratio may be expressed in terms of volts (rms) per division, decibels per division, watts per division, or any other specified factor.

Display Reference Level. A designated vertical position representing a specified input level.

NOTE

The level may be expressed in decibels (e.g., 1 mW), volts, or any other units.

Sensitivity. Measure of a spectrum analyzer's ability to display minimum level signals, at a given IF bandwidth, display mode, and any other influencing factors, and expressed in decibels (e.g., 1 mW).

Equivalent Input Noise Sensitivity. The average level of a spectrum analyzer's internally generated noise referenced to the input.

Display Flatness. The unwanted variation of the displayed amplitude over a specified frequency span, expressed in decibels.

Relative Display Flatness. The display flatness measured relative to the display amplitude at a fixed frequency within the frequency span, expressed in decibels.

NOTE

Display flatness is closely related to frequency response. The main difference is that the spectrum display is not recentered.

Frequency Response. The unwanted variation of the displayed amplitude over a specified center frequency range, measured at the center frequency, expresed in decibels.

Display Law. The mathematical law that defines the input-output function of the instrument.

NOTE

The following cases apply:
1) Linear—A display in which the scale divisions are a linear function of the input signal voltage;

2) Square law (power)—A display in which the scale divisions are a linear function of the input signal power;

3) Logarithmic—A display in which the scale divisions are a logarithmic function of the input signal voltage.

Dynamic Range. The maximum ratio of the levels of two signals simultaneously present at the input which can be measured to a specified accuracy.

Display Dynamic Range. The maximum ratio of the levels of two non-harmonically related sinusoidal signals each of which can be simultaneously measured on the screen to a specified accuracy.

Gain Compression. Maximum input level where the scale linearity error is below that specified.

Spurious Response. A response of a spectrum analyzer wherein the displayed frequency does not conform to the input frequency.

Hum Sidebands. Undesired responses created within the spectrum analyzer, appearing on the display, that are separated from the desired response by the fundamental or harmonic of the power line frequency.

Noise Sidebands. Undesired response caused by noise internal to the spectrum analyzer appearing on the display around a desired response.

Residual Response. A spurious response in the absence of an input signal. (Noise and zero pip are excluded.)

Input Impedance. The impedance at the desired input terminal.

NOTE

Usually expressed in terms of VSWR, return loss, or other related terms for low impedance devices and resistance-capacitance parameters for high impedance devices.

TERMS RELATED TO DIGITAL STORAGE FOR SPECTRUM ANALYZERS

Digitally Stored Display. A display method whereby the displayed function is held in a digital memory. The display is generated by reading the data out of memory.

Digitally Averaged Display. A display of the average value of digitized data computed by combining serial samples in a defined manner.

Multiple Display Memory. A digitally stored display having multiple memory sections which can be displayed separately or simultaneously.

Clear (Erase). Presets memory to a prescribed state, usually that denoting zero.

Save. A function which inhibits storage update, saving existing data in a section of a multiple memory (e.g., Save A).

View (Display). Enables viewing of contents of the chosen memory section (e.g., "View A" displays the contents of memory A; "View B" displays the contents of memory B).

Max Hold (Peak Mode). Digitally stored display mode which, at each frequency address, compares the incoming signal level to the stored level and retains the greater. In this mode, the display indicates the peak level at each frequency after several successive sweeps.

Scan Address. A number representing each horizontal data position increment on a directed beam type display. An address in a memory is associated with each scan address.

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

TEKTRONIX MANUAL CHANGE INFORMATION

Date: May 23, 1983
Product: 492/492P Spectrum Analyzer Service Vol. 1
Manual Part No.:   070-3783-01
Change Reference: C23/583

                           DESCRIPTION
==

                          TEXT CHANGES

ADD to Section 1, GENERAL INFORMATION AND SPECIFICATION, Page 1-18,
after the description for Option 08, before the description of
Option 20:

                      OPTION 11 (492P ONLY)

Provides front-panel automatic peaking for 492P's ordered with
Option 01, 02, 03, or 492P's with Option 01, 02, 03, 08.

ADD to Section 3, CALIBRATION-Performance Check, Page 3-7, before
the end of the functional check of front-panel controls and
pushbuttons, after EXTERNAL MIXER/PEAKING:

492P Option 11 Only.   AUTO PEAK/ EXT MIXER.   Pressing AUTO PEAK
runs an automatic peaking routine once, then sets the peaking
setting to the value obtained.   The manual PEAK knob is disabled.

The signal to be peaked must be within the center two horizontal
divisions.   Connect a cable from the 2nd LO output to the RF
INPUT, and tune to the signal at 2182 MHz.   Span down to 10
MHz/DIV, and center the signal.   Press AUTO PEAK and note that
PEAKING is displayed on the crt, and several sweeps are taken
with varying peaking settings.   After a number of sweeps, the
normal readout returns, and the signal is peaked.   Change the
frequency range to another band, then back to Band 2.   Note that
the signal is still peaked.

Pressing SHIFT EXT MIXER will switch to the external mixer mode.
See the EXTERNAL MIXER/PEAKING description.   Note that AUTO PEAK
also works for external mixers.

ADD to Section 5, THEORY OF OPERATION, Page 5-63, at the end of
the second paragraph under Mixer Bias Driver:

492P Option 11 Only.   The Programmable Bias, which sets external
mixer bias, or preselector tracking, is set by the data loaded
into DAC U3022, by the microcomputer, or by the front-panel
MANUAL PEAK control. The MANUAL PEAK control is connected to the
input of U2018 when the Q4 line of U4024 goes low and turns Q3019
on.   When MANUAL PEAK is selected, the DAC output is set for 0 ma.

                          Page 1 of 1

DESCRIPTION

==

TEXT ADDITIONS

Add to Section 1, GENERAL INFORMATION AND SPECIFICATION, Page 1-20, before the description for the Options for Power Cord Configuration:

OPTION 41

Option 41 (formerly Custom Mod UB) provides enhanced measurement capability for certain types of pulse-modulated signals used in Digital Microwave Radio. These include:

- A wider bandwidth preselector for better signal symmetry in the digital radio bands.

- A narrow 30 Hz Video Filter for resolution bandwith setting of 100 kHz (approximately 1/3000 of the resolution bandwidth) to improve amplitude variation analysis at specific frequencies and frequency spans unique to the digital radio measurements.

- Improved frequency span/div accuracy at 5 MHz/Div span to enable accurate signal band-width measurements.

Table 1-6

Characteristic	Performance Requirement	Supplemental Information
Frequency Span/ Div at Center Frequency of 6 and 11 GHz	5 MHz/Div is within +0, -1% over the center 6 divisions of the display	30 MHz equals 6.00 to 6.06 divisions.

Add to the Adjustment Procedure, Page 3-52, after step e-3:

For instruments with Option 41, omit step e-4 and e-5.

Add to the Adjustment Procedure, Page 3-53, after step g-5:

h. For instruments with Option 41, add the following:
   1) Switch to Band 4 (5.4-18 GHz) and tune Center Frequency to
      6 GHz. Set SPAN/DIV to 5 MHz.

   2) Modulate the Comb Generator with 0.2 μ markers from the
      time mark generator.

   3) Adjust R1071 (Fig. 3-31) for 1 marker/division +0, -1% over
      the center six divisions (30 Hz is no less than 6 divisions
      or more than 6.06 divisions),

   4) Tune the Center Frequency to 11 GHz and check span/div accu-
      racy. If necessary adjust R1071 so the span/div is within
      specifications at both center frequencies.

   5) Return the 492 FREQUENCY RANGE to band 1.

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: __5-2-84__   Change Reference: __C101/584__

Product: __492/492P Service Volume 1__   Manual Part No.: __070-3783-01__

| DESCRIPTION | Product Group 26 |

Page 1-19, after Option 32 , ADD:

OPTION 42

In Option 42 instruments the MARKER/VIDEO input port on the rear panel is replaced with an 110 MHz IF output port. It provides a signal with a bandwidth greater than 5 MHz, which makes the spectrum analyzer suitable for broadband swept-receiver applications.

ELECTRICAL CHARACTERISTICS

Characteristic	Performance Requirement	Supplemental Informatio
110 MHz center frequency	108. 5 MHz-111. 5 MHz	
3 dB bandwidth	>5 MHz	
bandpass ripple	</=0. 5 dB	
symmetry about 110 MHz	+/-1. 0 MHz	
power output with -30 dB input and signal at full screen (band 1)	</= 0 dBm	nominal output impedanc 50 ohm / in MIN DISTORTION mode only
(band 5)	>/= -40 dBm	1 dB compression of output >/= 0 dBm

Page 3-2, under Equipment Required for the Performance Check, CHANGE the recommendation for Spectrum Analyzer to read:

TEKTRONIX 7L14 Option 39 or 492/492P (used to adjust 1st and 2nd LO frequency offset and Option 42.

.J0-2775-00D

Product: __492/492P Service Vol. 1__ Date: __5-2-84__ Change Reference: __C101/584__

DESCRIPTION

Page 3-3, ADD to Equipment Required for the Performance Check:

ital Frequency Counter	10 Hz to 1 GHz, 20 mV sensitivity	TEKTRONIX DC503A Digital Counter
acking Generator with logic cable	Frequency Range 100 kHz to 1.8 GHz	TEKTRONIX TR502 (used to check Option 42)
RF Cable Assemblies		Tektronix Part No 012-0649-00

ge 3-3, ADD to Equipment Required for the Adjustment Procedure:

O Ohm Termination		011-0049-01
Bnc-SMB Flexible Cables		

Page 3-41, ADD after the 492P Verification Program:

For Option 42 instruments. Check Power Output at the 110 MHz OUT nnector on Band 1 (</= 0 dBm)

   a. Using the flatness data for the instrument being tested, find the signal th the highest amplitude.

   b. Connect a signal generator to the frequency determined in step a and wer level to -30 dBm.

   c. Set the 492/492P Option 42 REFERENCE LEVEL to -30 dBm and RF ATTENUATION o 0 dB.

   d. Keeping the signal centered with the CENTER FREQUENCY control, switch the FREQUENCY SPAN/DIV to 0 (the crt FREQ SPAN/DIV will indicate 10 ms).

   e. Adjust the CENTER FREQUENCY control of the 492 Option 42 to center the signal displayed on the 7L14.

   f. Check that the 110 MHz IF OUT output power is </= 0 dBm.

For Option 42 instruments. Check Power Output at the 110 MHz OUT Connector on Band 5 (>/= -40 dBm)

   a. Using the flatness data for the instrument being tested, find the signal with the lowest amplitude on Band 5.

   b. Connect a signal generator capable of the frequency determined in ep a to the 492 Option 42 RF INPUT.

   c. Set the signal generator to the frequency determined in step a and e power level to -30 dBm.

DESCRIPTION

d. Set the 492 Option 42 REFERENCE LEVEL to -30 dBm and RF ATTENUATION to 0 dB.

e. Keeping the signal centered with the CENTER FREQUENCY control, switch the FREQ SPAN/DIV to 0 (the crt Freq Span/Div will indicate 10 ms).

f. Adjust the CENTER FREQUENCY control of the 492 Option 42 to center the signal displayed on the 7L14.

g. Check that the 110 MHz IF OUT output power is >/= -40 dBm

30. For Option 42 instruments. Check Bandwidth (>5 MHz), Center Frequency (109.5 MHz-111.5 MHz), Bandpass ripple (</=0.5 dB), and Symmetry about 110 MH (+/- 1.0 MHz)

a. Connect the test equipment as shown in Fig. 3-21A.

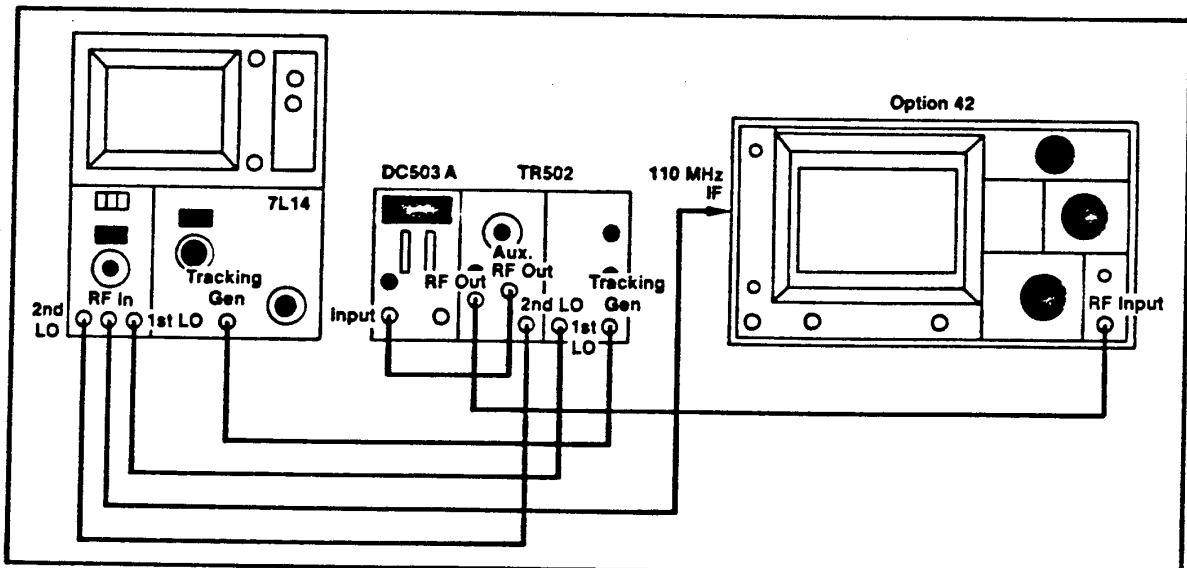
Fig. 3-21A

b. Set the instrument front-panel controls as follows:
   TR502   Output level -dBm   30
            Var dB   0
            Dot intensity   off

DESCRIPTION

7L14	Center frequency	0110
	Freq span/div	1 MHz
	Hz Resolution	3 MHZ
	Reference level	0 dBm
	Reference level mode	2 dB/Div
	Digital storage	off
	Time/Div	manual
	Triggering	
	Source	free run
	Mode	norm
	Video filter	on
DC503A	Function	Frequency A
	Timing	10 ms
	Channel A	
	Attn	X1
	Coupl	dc
	Source	ext/50 ohm
	Adjust level for a stable display (approx. 110.00 MHz)	

492/492P Option 42

REFERENCE LEVEL	-30 dBm
CENTER FREQUENCY	110 MHz
FREQUENCY SPAN/DIV	1 MHz
Hz RESOLUTION	1 MHz
VERTICAL DISPLAY	2 dB/DIV
MIN RF ATTEN	0 dB

c. Set the 7L14 Time/Div to Mnl and adjust the dot to center screen with the Manual Scan control.

d. Adjust the 7L14 Center Frequency control for an indication of 110.0 on the Frequency Counter.

e. While keeping the signal centered with the CENTER FREQUENCY control, set the 492 Option 42 FREQUENCY SPAN/DIV control to 0 (the Frequency Span/Div on the crt will indicate 10 ms).

f. Set the 7L14 Time/Div for a calibrated display and adjust the Reference Level and TR502 Var dB for full screen signal.

g. Switch the TR502 Dot Intensity to "on", and adjust the 7L14 Center Frequency for an indication of 110.0 on the Frequency Counter.

h. Check the bandwidth at a point 3 dB (1.5 divisions) from the peak of the signal to be >/= 5 MHz.

i. Check that any ripple present on the waveform is </= 0.5 dB (</= 0.25 divisions).

j. Check that the waveform symmetry is +/- 1.0 MHz (+/- 1.0 division) by assuring that the 3dB and 6dB points on the waveform are equidistant from center screen. (The peak of the signal may not be at center of the screen).

This concludes the Performance Check part of the Calibration Procedure.

DESCRIPTION

Page 3-80, ADD after the adjustment for Phaselock Calibration:

14. For Option 42 instruments. Adjustment of Option 42 Module. This adjustment need only be done after the circuit board in the module has been replaced.

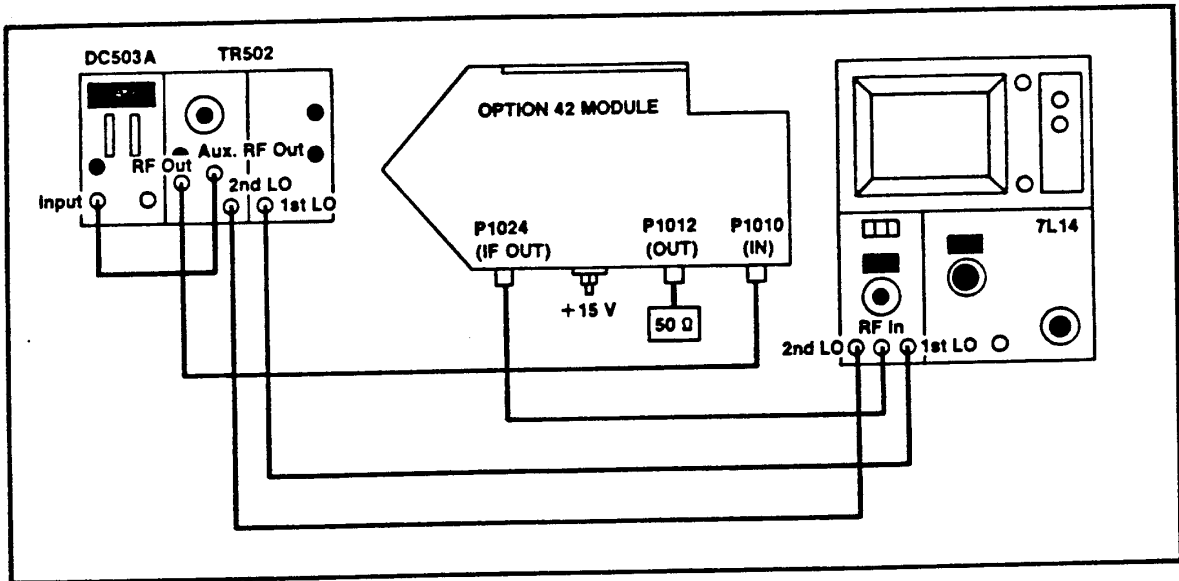   a. Connect the test equipment as shown in Fig. 3-55

Fig. 3-55

    b. Set the instrument front-panel controls as follows:

TR502	Output level -dBm	25
	Var dB	0
7L14	Center frequency	0110
	Freq span/div	2 MHz
	Hz Resolution	3 MHz
	Vertical display	2 dB
	Reference Level	0
	Display A and B	off
DC503A	Function	0.1 s
	Clock rate	1-1 us
	Ch A	
	depress	+ slope
	level	adjust as necessary

    c. Set the 7L14 Time/Div to Manual, and adjust the crt beam (dot) to center screen.

DESCRIPTION

d. The DC503A readout should indicate approximately 110.000 MHz. Adjust level as necessary, and adjust the 7L14 Center Frequency for an indication of 10.0 MHz.

e. Set the 7L14 Time/Div to calibrated display.

f. Adjust variable capacitors C1016, C1020 and C1024 for maximum amplitude, symmetry and bandpass (3dB and 6dB points).

   1. Adjust the bandwidth symmetry +/- 0.5 divisions (+/- 0.5 MHz) at the 3 dB and 6 dB points.

                    NOTE
         Check that points 3 dB (1.5 divisions) and 6 dB
         (3 divisions) down from the top of the signal
         are equidistant (+/- 0.5 divisions) from center
         screen.

   2. Check that bandwidth at the 3 dB point is 7.5 MHz, +/- 1.5 MHz.

   3. Check that any ripple present on the waveform is </= 0.2 div 0.4 dB).

                    NOTE
         A slight change in display may be observed when
         the cover is reinstalled on the module.

g. Check the Coupled Forward Gain (IF OUT port - P1024)

   1. Set the 7L14 Spectrum Analyzer Reference Level to 0 dBm.

   2. Check that the display on the 7L14 is between 4 and 7 divisions in amplitude (-5 dBm, +/-3 dBm).

h. Check the Input Compression.

   1. Set the TR503 Output Level and 494 REFERENCE LEVEL in one dB increments, to higher power level (-24 dbm, -23 dBm etc.)

   2. Continue changing the power level until the signal displayed by the 7L14 amplitude decreases (compresses 1 dB) 0.5 division.

   3. Check that the signal displayed on the 7114 indicates >/= 0 dBm

DESCRIPTION

i. Check Forward Gain

    1. Return the TR502 Output Level to -25 and remove the connection to the module IF OUT.

    2. Connect a 50 ohm termination to the IF OUT (P1024) connector.

    3. Connect the OUT (P1012) connector to the 7L14 RF Input with a 50 ohm cable.

    4. Adjust the 7L14 Reference Level until the displayed signal is near full screen (8 divisions).

    5. Check that the signal displayed on the 7L14 indicates -20dBm to -23 dBm (-21.5 dBm +/-1.5 dBm).

Date: 2-25-85
Product: 492 Ser.1   Manual Part No.: O7O-3783-O1
Change Ref: C102/285   Product Group: 26

DESCRIPTION

TEXT CHANGES

ADD on Page 4-1O, REPLACING ASSEMBLIES AND SUBASSEMBLIES in the
Maintenance Section, at the end of the procedure on Replacing the
Dual Diode Assembly:

  7. A procedure to adjust the First Converter Bias and Start Spur
Amplitude is provided in the Maintenance Adjustments section.

NOTE

> After replacement of the A12A1 Dual Diode Assembly
> in First Converter 119-1O17-O1, the 492/492P
> Spectrum Analyzer may not meet the flatness
> specification.
> After replacement of the A12A1 Dual Diode Assembly
> in First Converter 119-1O17-OO, the 492/492P
> Spectrum Analyzer may not meet the flatness or the
> start spur specification.

ADD on Page 4-35, after Troubleshooting Aids for the 2182 MHz Phase-
locked LO:

First Converter Bias and Start Spur Amplitude

NOTE

> After replacement of the A12A1 Dual Diode Assembly
> in First Converter 119-1O17-O1, the 492/492P
> Spectrum Analyzer may not meet the flatness
> specification.
> After replacement of the A12A1 Dual Diode Assembly
> in First Converter 119-1O17-OO, the 492/492P
> Spectrum Analyzer may not meet the flatness or the
> start spur specification.

Table 4-4A

EQUIPMENT REQUIRED FOR ADJUSTING FIRST CONVERTER BIAS
AND START SPUR AMPLITUDE

Test Equipment	Characteristics	Recommended Type
Digital Multimeter	$\leq$10 uV to $\geq$350 Vdc	TEKTRONIX DM502A and TM 500-Series Power Module
Sinewave Generator	2.0 MHz, 0 dBm +10 dBm to -100 dBm	TEKTRONIX SG503
Power Meter	must measure 0 dBm	Hewlett-Packard 435B
Power Sensor	must measure 0 dBm @2 MHz	Hewlett-Packard 8482A
Attenuator (13 dB)		TEKTRONIX 2701
Coaxial Cable (50 ohm)		Tektronix Part No. 175-2765-00
Coaxial Cable (50 ohm)		Tektronix Part No. 175-2337-00
Coaxial Cable (50 ohm)		Tektronix Part No. 175-3310-00

1. Preparation

    a. Remove the First Converter assembly from the spectrum analyzer, and connect the cables as shown in Fig.4-23A.
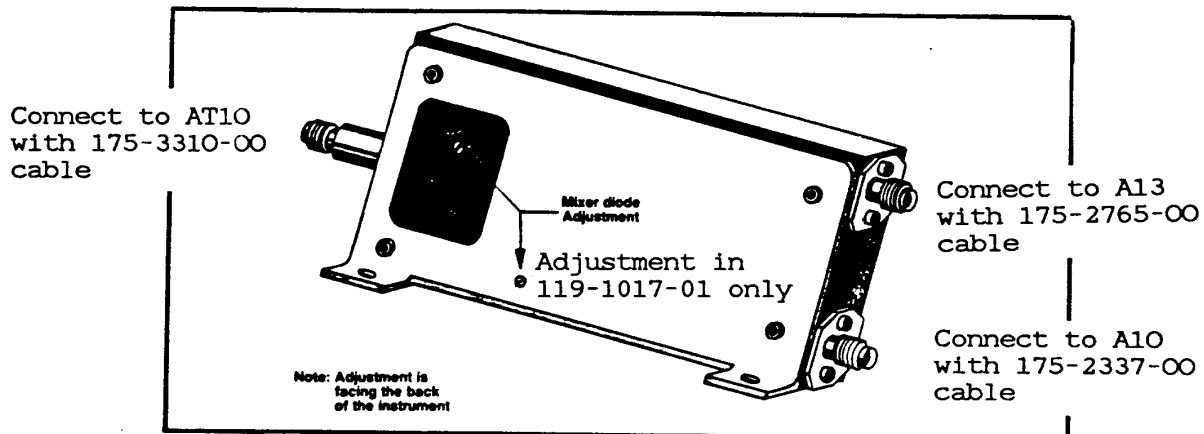

Fig.4-23A First Converter test equipment setup.

Page 2 of 5

b. Set the spectrum analyzer front-panel controls as follows:

TIME/DIV	AUTO
REFERENCE LEVEL	-30 dBM
FREQUENCY RANGE ▲	5.4-18 GHz (band 4)
FREQ SPAN/DIV	MAX
DIGITAL STORAGE	
DISPLAY A	off
DISPLAY B	off
MIN RF ATTEN	O
PEAK/AVERAGE	clockwise

c. Set the DM502 controls as follows:

Range Switch	20 DC Volts
DB pushbutton	out
Int pushbutton	out

d. Connect the DM502 red test lead to TP1011 on the 1st LO Driver board, and the black test lead to the instrument chassis, see Fig.4-23B.
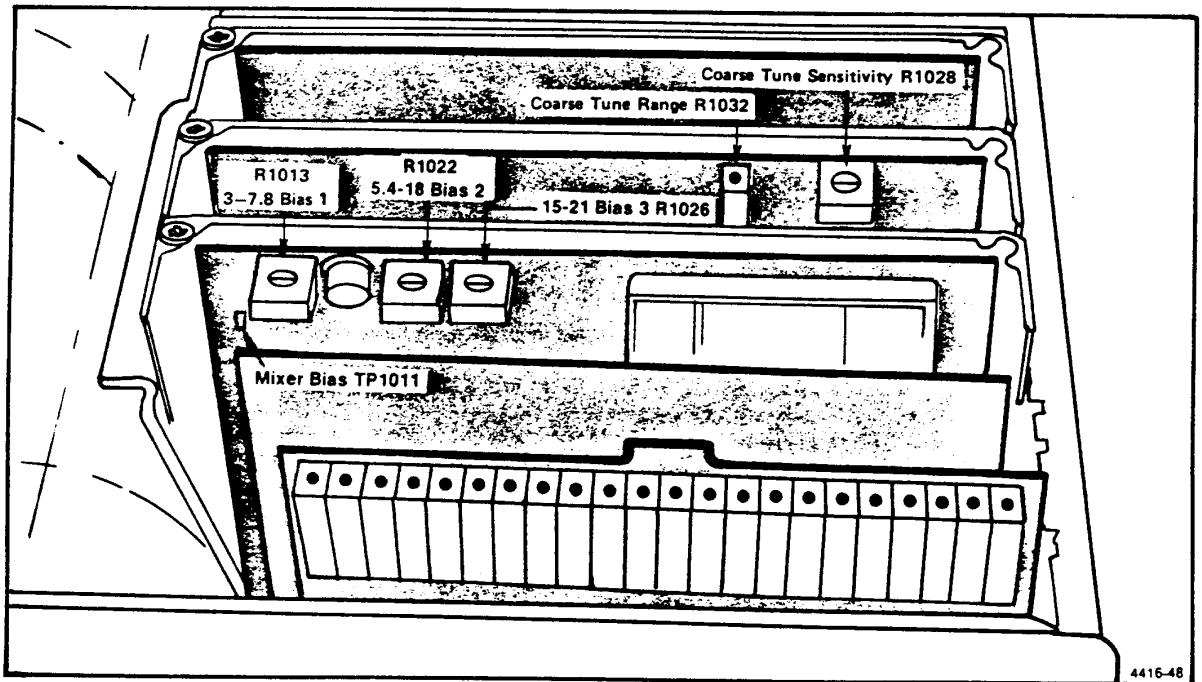

Fig.4-23B Adjustments and test points on the 1st LO Driver board.

Page 3 of 5

2. Bias Adjustment

a. Adjust R1022 (see Fig.4-23B) for a reading of -0.25 on the DM502.

b. Push FREQUENCY RANGE ▲ to band 5 (15-21 GHz), and adjust R1026 (see Fig.4-23B) for a reading of -0.25 on the DM502.

3. Start Spurious Amplitude and Band 1 Bias Adjustment.

a. Push FREQUENCY RANGE ▼ to band 1 (0-4.2 GHz), and adjust the CENTER FREQUENCY to 0 MHz.

b. Connect a 50 ohm cable from the SG503 Output to the 2701 Port 1/Input, and connect a second 50 ohm cable to the Power Sensor.

NOTE

Calibrate the Power Meter before making measurements.

c. Set front-panel controls as follows:

2701   0 0, DC

SG503
    Frequency Range   1-2.5
    Frequency Variable   for an indication of 2.00 MHz on the readout
    Amplitude Multiplier   x1
    Output Amplitude   counterclockwise

Power Meter
    Line   on
    Range   0 (on the dBm scale)

d. Adjust the SG503 Output Amp control for an indication of 0 on the Power Meter dBm scale.

e. Disconnect the Power Meter from the 50 ohm cable and connect the 50 ohm cable from the 2701 Port 2/Output connector to the 492 RF INPUT connector.

f. While keeping the 2 MHz signal centered with the CENTER FREQUENCY control, set the 492 FREQUENCY SPAN/DIV to 200 kHz.

g. Set the front-panel controls as follows:

2701   13 dB

492
    RESOLUTION BANDWIDTH   100 kHz
    VIDEO FILTER (WIDE)   on

h. Measure and record for reference the bandwidth of the 2 MHz signal at a point 6 divisions down from the top graticule line.

i. Adjust R1013 on the 1st LO Driver board for approximately -1.0 V at TP1011.

NOTE

During the following procedure, do not allow this voltage to go more positive than 0.1 V.

j. Bring the Start Spur signal to center screen with the CENTER FREQUENCY control. Frequency readout will indicate 0.00 MHz.

NOTE

For the least overall signal variations with frequency (flatness), the adjustments on the 1st Converter must be made in conjunction with R1013 (bias for bands 1, 2, and 3).

k. Alternately adjust R1013 and the adjustments on the 1st Converter (see Fig.4-23A) until the bandwidth, at the 6 dB point, matches the bandwidth of the previously displayed 2 MHz signal.

NOTE

It will be necessary to alternate between the above adjustments to decrease the amplitude of the start spur. While this is being done, assure that the voltage at TP1011 does not exceed +1.0 V.

It will not be possible to null the start spur to a point where the top of the signal will be on screen. To assure that the signal meets the specification (-13 dBm), the bandwidth is matched to the bandwidth of the previously displayed 2 MHz signal. Do not adjust the start spur lower than -13 dBm.

l. Remove all test leads from the test setup.

Page 5 of 5

                              DESCRIPTION
===
EFF SN B053575   Product Group 26
                         TEXT CHANGES   Revised 11-16-83

Calibration - Performance Check

Page 3-32, REPLACE the NOTE at the top of the page with the following:

                              NOTE
        Because of deflection amplifier response, the
        display amplitude will decrease at the high
        frequency end.

        The triggering signal can also be applied
        directly from the sinewave generator to the
        MARKER/VIDEO connector, if external video
        is selected by connecting a jumper between
        pins 1 and 5 of the ACCESSORIES connector.

Calibration - Adjustment Procedure

Page 3-47, REPLACE step 3b and 3c with the following:

b. Apply a 5 kHz, 0 to +4 V signal from the sinewave generator,
through a bnc cable to the MARKER/VIDEO input on the rear panel,
and connect pin 1 and pin 5 of the ACCESSORIES connector with
a pin-jack-to-pin-jack jumperwire.

c. Adjust Vert Gain, R1066 (Fig.3-23), for a full screen display
(0 to +4 V). Remove the 5 kHz signal from the MARKER/VIDEO input
and remove the jumperwire from the ACCESSORIES connector.

Calibration - Adjustment Procedure

Page 3-48, REPLACE step 4b with the following:

b. Apply 10 ms time marks from the time-mark generator to the
MARKER/VIDEO input, and connect pin 1 and pin 5 of the ACCESSORIES
connector with a pin-jack-to-pin-jack jumperwire, see Fig.3-28.
Connect the Trigger Output of the time-mark generator to the
HORIZ/TRIG input on the rear panel of the 492/492P. This should
provide a display of 10 ms markers.

                          Page 1 of 4

Calibration - Adjustment Procedure

Page 3-58, REPLACE the entire Step 8 with the following:

8. Baseline Leveling (Video Processor)

    This procedure adjusts the baseline so Band 1 and 4 response perturbations are offset to level the display.

    a. Test equipment setup is shown in Fig. 3-35. The output of the sweep generator is applied through a 3 db attenuator and high-performance coaxial cable to a power divider. Connect one output of the power divider directly to the RF INPUT of the 492/492P and the other to the sensor for the power meter. Set the RF plug-in ALC switch to the MTR position, and connect a coaxial cable between Recorder Output of the power meter and the Ext ALC Input of the plug-in unit on the sweeper. Set the Power Level to approximately -10 dBm, then adjust the Gain on the unit for stable operation (output stops oscillating).

    b. Set the FREQUENCY to 100 MHz, FREQ SPAN/DIV to 5 MHz, REF LEVEL to -20 dBm, TIME/DIV to AUTO, and activate AUTO RESOLN and 2 dB/DIV.

    c. Apply the CAL OUT signal to the RF INPUT, and adjust REF LEVEL for an on-screen display of approximately 6 divisions. Note the signal amplitude.

    d. Remove the Calibrator signal and apply the output of the sweep oscillator as shown in Fig. 3-35. Set the FREQUENCY to 1.8 GHz and apply a 1.8 GHz signal at -20 dBm, from the Sweep Oscillator to the RF INPUT. Note the amplitude of the 1.8 GHz signal. (It may be necessary to switch to 10 dB/DIV mode to observe the signal.

    e. Adjust Band 1 Slope R1012 so the signal amplitude equals that of the 100 MHz reference. R1012 is located on the Video Processor board next to high leveler adjustment R1013.

    f. On the Video Processor board, pull the Leveler Disable plug, P3035 (Fig. 3-36).

    g. Set the FREQUENCY to 10 GHz, FREQUENCY RANGE to 5.4-18.0 GHz (Band 4), FREQ SPAN/DIV to MAX, REF LEVEL to -10 dBm, and TIME/DIV to 10 ms. Activate 10 dB/DIV and AUTO RESOLN.

    h. On the sweep oscillator, select a 5.5 GHz cw marker and adjust the output for a -10 dBm reading on the power meter.

    i. Activate 2 dB/DIV, and adjust the REF LEVEL so the signal amplitude is half screen. Adjust MANUAL PEAK for maximum response or activate AUTO PEAK.

j. On the sweep oscillator, change to the automatic internal sweep (Marker Sweep) and set the sweep time for 100 s/sweep (its slowest sweep).

k. Activate VIEW A and VIEW B, then select a sweep time on the 492/492 so the stored display is solid (no breaks in the digitized display, Fig. 3-37A).

l. Activate MAX HOLD. Trace and record the response of Band 4. Activate SAVE A.

m. Deactivate VIEW A and MAX HOLD (SAVE A and VIEW B are still active).

n. Activate 10 dB/DIV and note the baseline. Activate NARROW Video Filter, and adjust the REF LEVEL so the baseline moves to the top of the screen.

o. Press 2 dB/DIV and VIEW A, then adjust the REF LEVEL so the SAVE A display and the baseline are at center screen.

p. Unplug P2060 (Fig. 3-36) and move it from the Normal to Invert mode position (one pin to the left). Replace Leveler Disable plug P3035.

q. Start with R1061 and adjust the leveling potentiometers sequentially, from R1061 through R1013, so the contour of the baseline is an average of the SAVE A display. In the process, use Horiz adjust R1069 (Fig. 3-36) to shift the baseline to the right or left so the baseline aligns with the average contour of the SAVE A display.

r. Replace P2060 to the Normal mode position (one pin to the right). The baseline will now be 180 degrees or the inverse of its previous position.

s. Deactivate and then activate VIEW A, VIEW B, SAVE A, and MAX HOLD. Retrace and check new response. Response should appear flat (Fig. 3-37B).

t. Disconnect and remove the signal to the RF INPUT from the test equipment.

u. Compensation adjustment R1065 is set at the factory and usually does not require adjustment. Pull Leveler Disable plug P3035, then replace it. If the baseline remains straight or breaks up after the plug is replaced, compensation is required. The adjustment procedure is as follows.

----

(1) With the front-panel controls set as directed in part b, activate the NARROW Video Filter and change TIME/DIV to 50 ms. Alternately turn the 19 level adjustments clockwise and counterclockwise so every other potentiometer is fully clockwise and the adjacent potentiometer is fully counterclockwise. The display should now appear as a periodic triangular waveform.

(2) Adjust the REF LEVEL so the baseline is near full screen, then switch on the 2 dB/DIV mode and adjust so the display is mid-screen (Fig. 3-38A).

(3) Turn Compensation adjustment R1065 counterclockwise until the display breaks up (Fig. 3-38B).

(4) Now, turn R1065 clockwise 1.5 to 2 turns past the point the display again becomes a periodic triangular waveform.

(5) Turn Horiz adjustment R1069 to center the display.

(6) Return the baseline leveler adjustments to their midrange position for a straight line display, and proceed with the baseline leveling alignment as previously described (parts a through t).

TEKTRONIX MANUAL CHANGE NOTICE

Date: 2-12-85
Product: 492/492P Service Vol 1.   Manual Part No.:   070-3783-01
Change Ref: M55287   Product Group: 26

DESCRIPTION

EFF SN B055508

REPLACE the description of the Digital Control on Page 5-69,
Track/Hold Amplifiers on Page 5-70, and Write-Back Circuits on Page
5-70, all in the Theory of Operation Section, with the following:

Digital Control

The digital control circuits consist of buffer U4035, address decoder
U4045, steering register U4025, and the steering gates (U4015A, U4015B,
U4015D, U4060A, U4060B, and U4060D). Because of the quantity of data
that must pass through these circuits, a steering register is used that
has a separate address. The first byte of data, which is the steering
byte, is clocked into U4025 by the ADDRESS 70 signal. The output
levels are applied to the steering gates, and the circuit waits for
the next byte. The microcomputer then furnishes the first byte of
data to be sent to low-order fine-tune digital-to-analog converter DAC,
for example, by way of storage register U3015. The byte is clocked
into the register by the coincidence of low states at the inputs of
U4015B; one from the steering byte, and the other from ADDRESS 71
signal, which is used to clock the steered data bytes into the correct
register. This continues until seven bytes of data have been clocked
into the correct register, including the steering byte. The third
output from U4045, ADDRESS 80, controls transistors Q1058 and Q2017,
which enable the write-back function.
In addition to the six steering lines that drive the steering gates,
U4025 also controls, by means fo the Q3 and Q7 lines, the hold/track
selector transistor for each converter side. Table 5-17 illustrates
the format for ADDRESS 70. Addresses are expressed as hexadecimal
numbers. Table 5-18 lists some of the significant states that are
used to tune the DAC.

Storage Registers. Six storage registers are used in the circuit,
U3015, U3025, U3035, U3050, U3060, and U3070. Since both sets are
identical, only the coarse tune section will be described.

Data from U4035, the data buffer, is clocked into the registers each
time a different tune voltage is required. U3050 feeds the lowest
eight bits to the low-order DAC, U2055; U3070 feeds the highest
eight bits of the high-order DAC, U2060. U3060 feeds the remaining
bits of both units.

Digital-To-Analog Converters. Since both the coarse and fine tune
circuits operate in the same manner, only the coarse tune section
of the board will be discussed here. Figure 5-28A is a functional
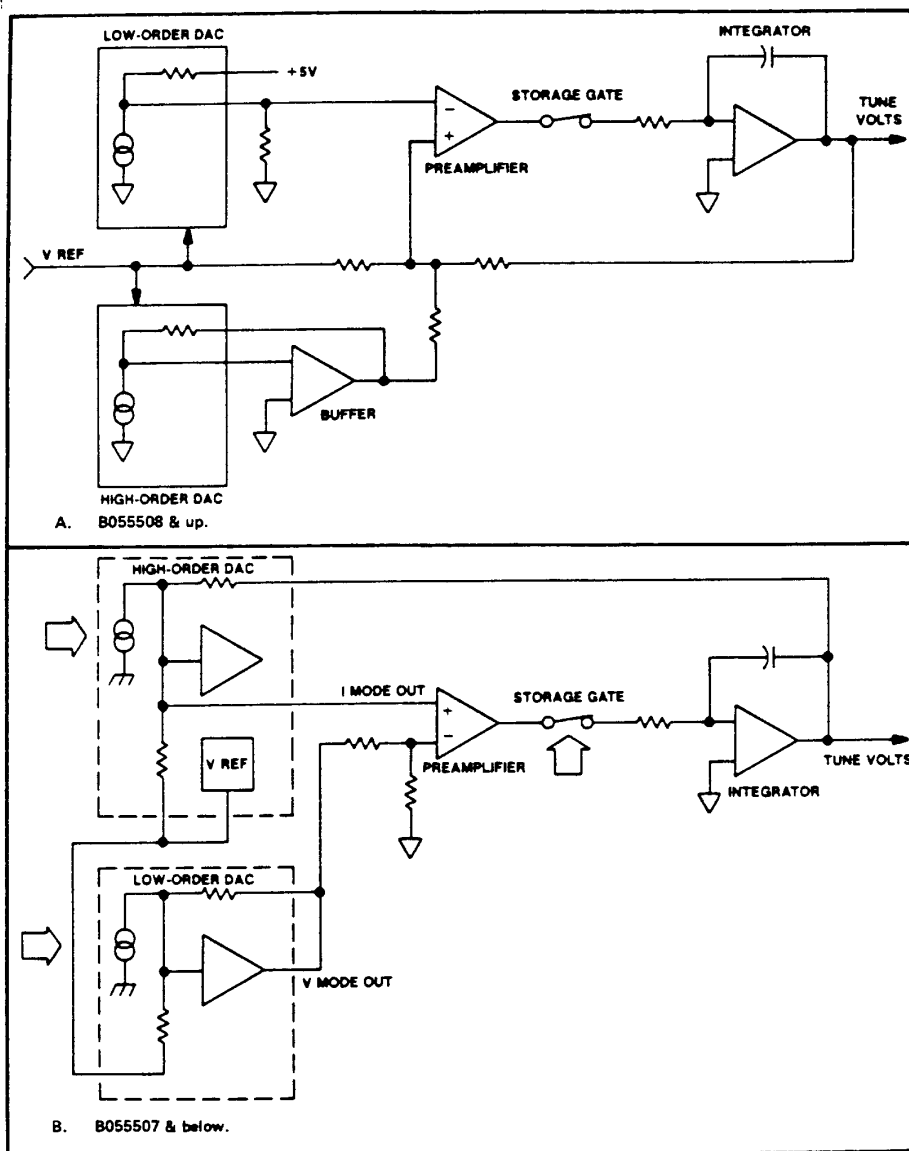block diagram of the circuit.

Page 1 of 6

Fig. 5-28   Basic tune voltage converter

Page 2 of 6

Each side of the converter has two DAC's summed together to produce
an output of approximately +/- 10V. The DAC's are programmable
current generators driving the preamplifier-integrator circuit.
The high-order DAC provides 0 - 2 ma of current to the circuit via
the buffer, while the low-order DAC provides approximately +/- 2.5 mV
at the inverting input of the preamplifier. The preamplifier then
drives the integrator via the storage gate.

Since the converters provide the DC voltages to tune the oscillators in
the instrument, moise and extraneous signal susceptibility must be kept
to a minimum, hence the isolated ground system for each half of the
circuit.

Track/Hold Amplifier

The amplifier consists of high-order DAC U2060, low-order DAC U2055,
buffer U2050, preamplifier U1065, storage gate FET Q1065, and
integrator U2070.

The circuit output is required to tune approximately +/- 10V for the
full-scale range of U2060. When U2060 is off and U2050's output is
at 0V, the +10V output level is set by the 1 ma of current in R1055,
and the combination of R1032, R1053, and R1070. When U2060 is fully
on, and U2050's output is at +10V, the -10V output level is set by
the 2 ma of current in R1052, minus the 1 ma constantly flowing in
R1055. Full-scale gain is adjusted by R1032. R1052, R1053, and
R1055 are TC matched to minimize output voltage drift as a function
of temperature. Low-order DAC U2055 tunes approximately +/- 2.5mV
at pin 1, and its gain is adjusted by R1028. The gain of preamplifier
U1065 is set at about 10,000 by R1056 and the 5 Ohm combination of
R2059 and R2060. The combination of CR1056, CR1058, R1054, and
R1059 limits the gain of U1065 when the output exceeds approximately
0.7V in either direction.

U1065 is connected to integrator U2070 via storage gate FET Q1065,
which is on in the Track mode. Q1065 is turned off any time one of
the DAC's is being tuned to allow its output to settle before tuning
U2070's output. It is also turned off during the interval when a
carry from the low-order DAC to the high-order DAC is being
accomplished. Q1065 is controlled by Q1061. When Q1061 is on,
CR1064 is back-biased. The voltage at the gate of Q1065, which is
developed by R1064, R1065, R1066, and R1067, is near 0V and Q1065
conducts. When Q1061 is off, sufficient voltage to pinch off Q1065
is applied through R1062 and CR1064.

Page 3 of 6

U2070 tracks the output of U1065 when the circuit is in the track mode and serves as the inverting amplifier in the feedback system shown in Figure 5-28. Normally the incoming signal is routed through R2067. To improve the integrator's slewing rate, CR1067 and CR1069 conduct and connect R1068 across R2067 when input signals in excess of 1V are present.

Write-Back Circuit

This circuit consists of comparator U1055 and enabling transistor Q1058. When it is necessary to do a carry between the low and high-order DAC's, the circuit is put into the hold mode by turning off Q1065. U2060 is incremented one bit and U2055 is reset to all 0's. The output of U1065 is now at something other than 0V. The purpose of the following approximation routine is to get U1065's output as close to 0V as possible before switching the circuit back into track mode by turning on Q1065. Comparator U1055 detexts whether U1065's output is above or below coarse tune ground. The instrument microcomputer begins to exercise the low-order DAC bits one at a time from MSB to LSB. After each bit is turned on, U1055 is enabled by turning off Q1058. If U1055 detects that U1065's output has crossed 0V, that bit is turned off and the next lower bit is turned on. This continues through all 12 bits and when completed, should have U1065's output very close to 0V. Q1065 can now be turned back on without causing excessive signal jump on screen.

-10V Reference Buffer

The circuit uses the voltage reference developed on the 1st LO Driver board as a reference for the DAC's. Differential amplifier U2045 receives the -10V reference and -10V reference return and removes any common-mode signals present. Resistor pairs R1048-R1049 and R1050-R1051 are TC matched to minimize reference voltage drift over temperature.

ADD to Page 4-5 in the Maintenance Section, after the paragraph
on Diode Checks:

Surface-Mounted Components

Surface-mounted components (SMC's) have been used in this instrument.
These SMC's are mounted directly onto the circuit board, rather than
through holes in the PCB. Electrode configuration of these components
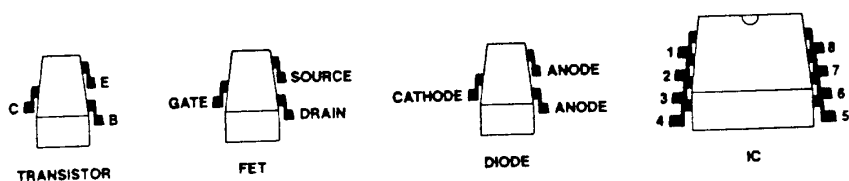is shown in Fig.4-4A.

Fig. 4-4A. Electrode configuration for Surface-Mounted Components.

The positive end of electrolytic capacitors is identified with a band.
Other capacitors and resistors have no visible identification, though
their value can be measured with an Ohm Meter or a Capacitance Meter.

Surface-mounted semiconductor devices are statically sensitive, and
should be treated as outlined in the beginning of this section.

Replacement. A Hot Air Machine, such as Hart Model 200A manufactured
by Nu-Concept Computer Systems Incorporated of Colmar, Pennsylvania,
is recommended for unsoldering and soldering surface-mounted
components.

Another method to remove and solder SMC's is by hand, using a hot air gun and a pair of tweezers.

    1. Unsolder the component. Do not apply too much heat. The pad connecting the device to the circuit board may be lifted.

    2. Clean the board with isopropyl alcohol.

    3. Solder the SMC. SMC's are pretinned, and should be soldered onto the board with solderpaste rather than solder.

CAUTION

If you use a soldering iron, use one with a small tip. After applying the solderpaste, touch the corner of the pad with the iron to fasten the component. Avoid touching the component with the hot soldering iron. Thermal shock causes hairline cracks that are not visible to the eye.

NOTE

Solderpaste has a shelflife of 3 months when stored at room temperature. It can be used up to six months if it stored under refrigeration.

Solderpaste should be at roomtemperature before use.